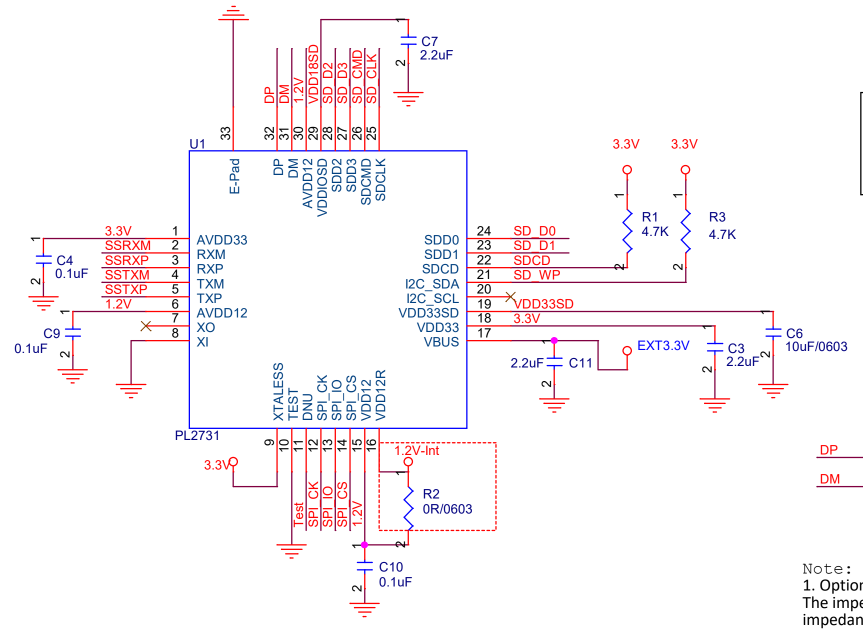
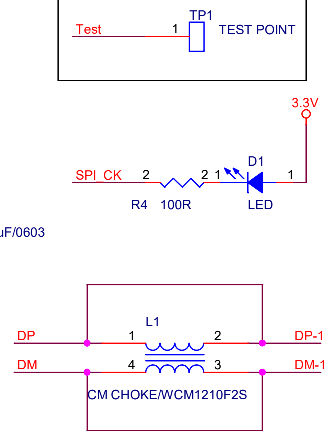
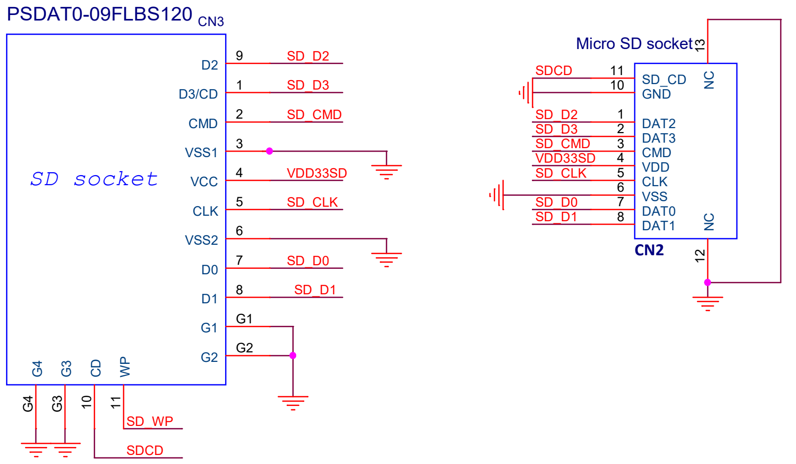


For F/W debugging



Note:
1. Optional L1 for reducing EMI of USB2.0 signal.
The impedance of the choke depends on the impedance of USB2.0 trace on PCB

2. L1 do not be applied because they are bypassed in the schematic. If PCBA can't pass for EMI test, it is needed to cut the byapss trace(for short of them) and apply them for EMI reduction.
(因不一定需要choke才能通過EMI認證，故此電路已先將CM choke旁路，EMI初測時不需焊接choke，若EMI無法通過測試，再將旁路的走線割除並焊接choke)

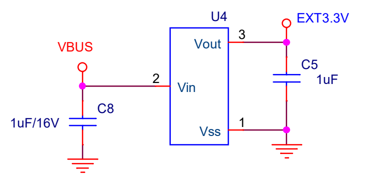


Note:
1.If in write protection(WP) mode, WP pin is floating if it is not pulled-up.
If not in WP mode, WP pin is low level(GND).

2. If card inserted, CD pin is low level(GND)

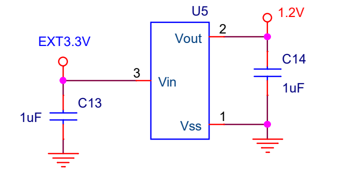
5 - 3.3V LDO

A6301A/5-3.3V LDO/min. 250mA/SOT89-3



Optional 3.3 - 1.3V LDO

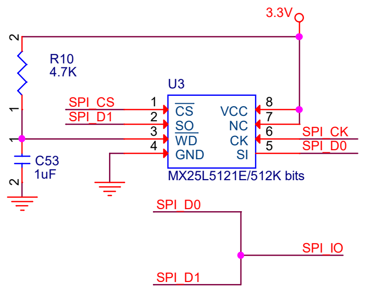
A6301A/3.3-1.3V LDO/min. 150mA/SOT23



1.2V output should be 1.28~1.31V

Note:
1.For reducing the operational temperature of PL2731 at USB3.0 mode.
2. If U5 is applied, R2 should be not applied(NC).

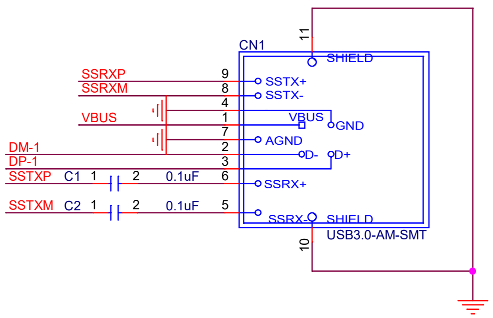
Optional SPI Flash



Note:
1.For FW updating, customized product info. such as PID, VID...

2.If you need write protection(WP) function, you need to use external FW in SPI flash because internal FW can't support WP.

3.Please contact FAE for detailed supported flash list.



Title	PL2731_SD & uSD Reader_USB3.0-A+2-LDO
Size: B	Document Number: <Doc> — Rev: 1.9
Date: Tuesday, April 21, 2020	Sheet 1 of 1