PL2561

USB 2.0 to UART and SPI controller

PCB Layout Guideline

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Overview

The guidelines provide the recommended consideration on PCB layout.

1. USB2.0 trace

- USB2.0 differential pair traces should be routed with differential impedance of 90±15% ohms.

- The trace length of one trace of USB2.0 differential pair should be as the same as possible with another trace. Maximum trace length difference of USB2.0 differential pair should be no greater than 100 mils.

- Avoid the signal traces with the angle of 90 degrees as Figure 1. The signal traces include the traces of USB2.0 signal and crystal.

Figure 1

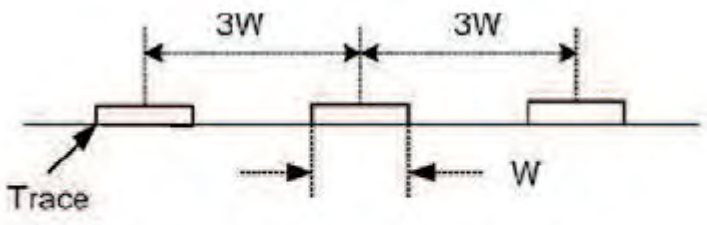
- When using a common mode choke and an ESD protection part to suppress EMI and ESD, they should be placed as close as possible to the USB connector.

- Never route USB2.0 differential traces near other high frequency traces and parts such as crystal and IC to avoid crosstalk.

  Ways to Avoid Crosstalk:

  -Use the 3W rule (3 times of the width of USB2.0 signal trace as Figure 2) to separate USB2.0 signal trace from other high frequency traces and parts.

  -Use ground traces/guards around either USB2.0 signal trace or other high frequency signal traces and parts.



The "3W" rule

Figure 2

- Never route USB2.0 differential traces near the PCB edge to prevent from the distortion of USB2.0 signal by EMI and ESD.

- Never route USB2.0 differential traces over the split ground and power planes as Figure 3. For a worse example as Figure 3, USB2.0 differential traces are routed on the top layer of PCB and overlapped a split ground or power planes with other signal traces on the second/ adjacent layer(for 4-layer PCB) or the bottom/adjacent layer(for 2-layer PCB) of PCB.

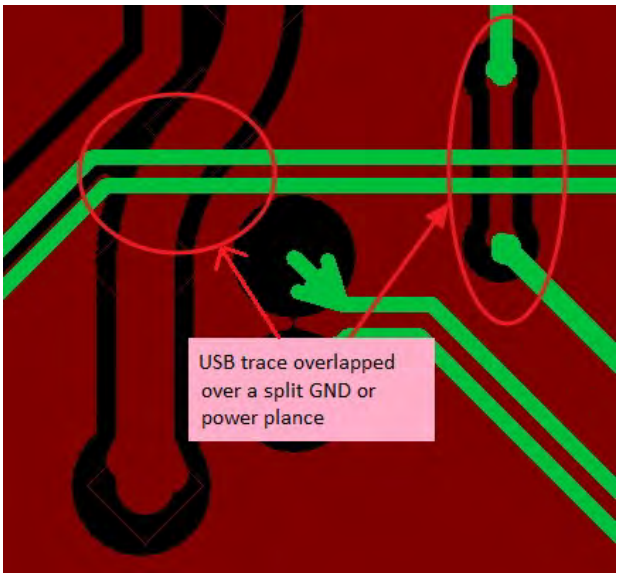


Figure 3

- It is recommended to straight route USB2.0 differential pair and less route them with bends as Figure 4.

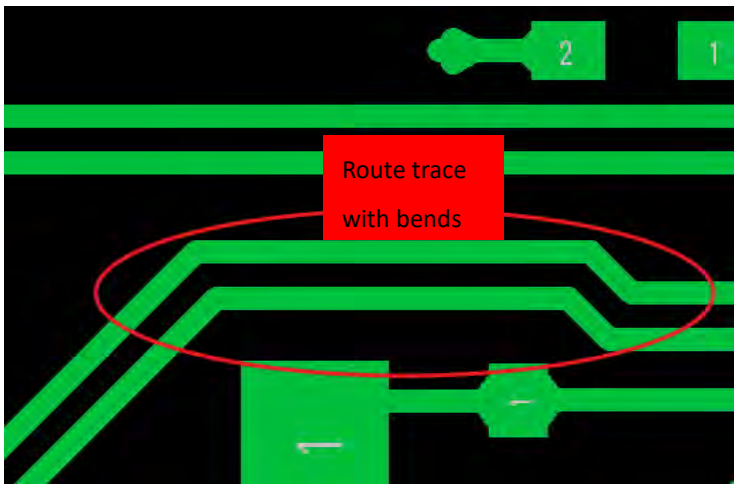


Figure 4

- Stubs on USB 2.0 differential pair as Figure 5 should be avoided. While stubs exist, it will cause signal reflection and affect signal quality. If a stub is unavoidable in the design, should be as shorter as possible.

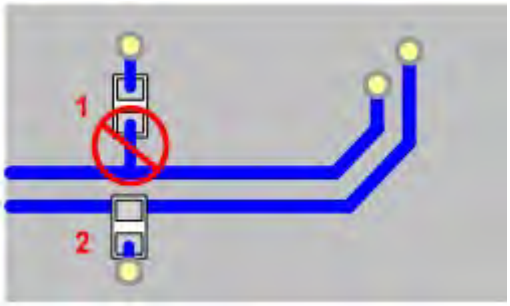


Figure 5

2. Power

- Place decoupling capacitors near the power pin of PL2561.
- Minimum trace width of 1.2V, 3.3V power is 10 mils for application without GPIO pins.
- Minimum trace width of VBUS power pin of USB connector and other 5V power pins is 20 mils.
- It is recommended to partition a 3.3V power plane to connect all of 3.3V power nets if there are many 3.3V power nets in your schematic.

3. SPI

- The SPI-bus traces should be length matched. Maximum trace length mismatch should be no greater than 150 mils.
- Route the clock trace at least 3x of the trace width away from all other signal traces as Figure 2.
- Use as less via(s) as possible for clock trace.
- Route the SPI-bus traces as straight as possible as Figure 1. Stubs on SPI-bus traces as Figure 5 should be avoided.
- Route SPI-bus away from other clock traces and noisy power supply components such as the inductors of DC-DC converter.
- Route the SPI-bus traces on continuous ground in the next layer as possible for reference plane as Figure 3.

4. Others

- The trace between crystal pins of PL2561 IC and the external crystal is as short as possible.
- NC pins of 4-pin crystal should be connected to GND to prevent from generating EMI.
- Allocate the unused area of PCB as a GND plane to enlarge GND plane on whole PCB.

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