PL2561 USB 2.0 HID-to-UART/I²C/SPI Controller

USB Interface

- Fully compliant with USB 2.0 specification
- USB Human Interface Device (HID) class:
  - No driver installation needed for Windows, Mac, Linux, and Android.
  - Provides HID-to-UART/I²C/SPI SDK(DLL libraries)for application development.
- UHCI/OHCI (USB1.1), EHCI (USB2.0), and xHCI (USB3.X) host controller compatible
- Highly integrated USB 2.0 High-Speed and Full-speed transceiver with built-in pull-up resistor and reference resistor to reduce PCB external component
- Support on-chip MTP for customization of USB device, configuration, and serial number ,descriptors, no need of external memory
- Each IC has unique ID (for serial number)
- Support bus-powered, self-powered and high-power USB configuration
- Support Windows USB selective suspend (remote wakeup enabled)
- Support VBUS detect function to attach USB host after VBUS is detected
- Supports 3.3V VBUS voltage operation
- Support read-only Mass Storage Device Class for file storage.

GPIO Interface

- Versatile GPIO functions and routing logic provides easy to use multi-IO functions
- Configurable output driving strength
- Total 9 GPIOs can be used
- Flexible GPIO configuration
- HBM ±6.0KV ESD protection

UART Interface

- Support a UART interface
  - TXD and RXD UART pins
  - Flexible baud rate up to 115200 bps
  - 5, 6, 7, or 8 data bits
  - Odd, Even, Mark, Space, None parity mode
  - One, one and half, or two stop bits
  - No Hardware flow control (No support by OS driver)
  - Software flow control (XON/XOFF)
- Individual 512bytes FIFO for IN/OUT buffer
- Configurable threshold of flow control
- Configurable invert option of UART signals
- Suspend pin control for RS232 transceiver

I²C Serial Interface

- Support I²C Master mode.
  - Two open-drain wires SCL and SDA.
  - Support I2C Standard mode, Fast Mode and Fast Mode Plus (FM+)
  - Support flexible I2C SCL clock generation, clock rate up to 1MHz.
  - 7-bit address support.
- Individual 512bytes FIFO for IN/OUT buffer
- Support remote wakeup via WAKEUP pin.
- Support HID over I2C specification

SPI Serial Interface

- Support SPI Master mode.
- Support clock rate up to 32MHz at VDDIOP2 >=1.9V
- Up to 1024-byte bi-directional data buffers
- Support clock polarity options (Inverse or

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- MM ±300V ESD protection
- Latch up ±200mA ESD protection

not).

- Support remote wakeup via WAKEUP pin.

Miscellaneous

- Integrated Power-on-Reset (POR) circuit
- Integrated 5V to 3.3V LDO that can support 100mA for chip internal and external components
- Independent and wide I/O voltage range (+1.8V ~ +5V) for port #0~2
- -40˚C to 85˚C operating temperature
  QFN32 package (RoHS compliant and Pb-free Green Compound)

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REVISION HISTORY

Revision	Description	Date
0.1	Initial release	2023-4-25
0.2	- Change max. baud rate as 12M bps in page 1 and 10. - Change min. baud rate as 5 bps in Table 9-9	2023-5-2
0.3	- Removed the following items in page 1 a. Configurable transmit and receive LED pins b. Optional clock output and PWM output - Change “5V to 3.3V LDO that can support **60**mA for **external components”** - Change pin10 as NC from PU, Type of pin9 as I/O, Type of pin16 as Output in Table 7-2 - Added pin18 as VDD12(1.2V input) in Table 7-4 - Change the default pin name of pin 17 and 19 as GPIO in Table 7-6	2023-7-10
0.4	-To change max. frequency of SPI clock as 32MHz in page 1 and 10 -To remove CLK/PWM function in Figure 4-1 -To change pin name of pin17and 19 as GPIO Figure 7-1 -To change ordering part number as PL2561A**2**FRG8P**1** -To update PL2561 Outline Diagram in Figure 10-1	2023-8-28
0.5	-To change **Factory default is VBUS_DET input pin** in table 7-3 as Factory default is **GPIO** input pin -To change **Factory default is SUSPEND_N output pin** in table 7-3 as Factory default is **GPIO** input pin	2023-10-3
0.6	-To change max. baud rate as 115200 bps and related description -To change total number of GPIO as 9 and related description -To change as only TXD and RXD pins from full UART pins (without HW flow control) and related description -To change GP1_3 and GP0_2~ GP0_7(HW flow control pins of UART) in Table 7-3 as default GPIO -To change NC pin and HW flow control pins of UART as GP1_3 and GP0_2~ GP0_7 and mark the Exposed Pad in Figure 7-1 -To change section 7.3 as **PL2561 chip provides a total of 9 configurable GPIO** -To change GPIO as IO pin in first column of Table 7-6 and add additional 7 GPIO pins and BC_DET , CLK, WAKEUP ,PWMA and PWMB to Table 7-6 -To add BC_DET ,CLK, WAKEUP ,PWMA and PWMB to Table 7-7 -To removed USB-IF Logo and TID in page4 and 9 -To change SD0 as SD0/MISO and SD1 as SD1/MOSI -To change the pin description of pin 18 and 21 in table 7-4 -To change SUSPEND_N as low active in table 7-7 -To change P3_10(pin19) as only support 3.3V in table7-3 -To add the remote wakeup function into the pin description of P0_7(pin 31) in table 7-3 -To change min. VIN as 4.0	2024-3-1
0.7	-To change the description of pin 1, 2 and 21 in table 7-4 -To change “Integrated 5V to 3.3V LDO that can support 60mA” in page 2 as “Integrated 5V to 3.3V LDO that can support 100mA for chip internal and external components” -To change the description of PWMA and PWB in table 7-7 -To add 9.7 Package Thermal Characteristics	2024-3-19
0.8	-To change “To change SD0 as SD0/M**I**SO and SD1 as SD1/M**O**SI” in the description of the revision history V0.6 as “To change SD0 as SD0/M**O**SI and SD1 as SD1/M**I**SO” -To change “the description of PWMA and PWB” as in the description of the	2024-4-3

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	revision history V0.7 as “the description of PWMA and PW**M**B” **-**To change the description of pin21 as +3.3V Power input in table 7-4	
0.9	- To Add “Support HID over I2C specification” and “at VDDIOP2>=1.9V” for max. 32MHz of SPI clock in page 1 - To change min. VDDIOP2 as 1.9V in Table 9-1 and 9-3 - To add 9.9 SPI Frequency Characteristics and Table 9-11: SPI Frequency Characteristics - To change the Figure in 10.1 and 11.1	2024-6-17

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1. Product Applications

- USB to I²C/SPI master controller
- USB to UART controller
- HID device class controller
- MCU-based devices to USB host interface
- Point-of-Sale (POS) Terminals/Printers/Pole Displays
- USB Barcode/Smart Card Readers
- PC I/O Docking Station/Port Replicators
- Healthcare/Medical USB Interface Data Transfer Cable
- Serial-over-IP Wireless Solution
- Cellular/PDA USB Interface Data Transfer Cable
- GPS/Navigation USB Interface
- Industrial / Instrumentation / Automation Control USB Interface
- Wireless / Zigbee USB Interface
- Set-Top Box (STB) / Home Gateway USB Interface
- Sensor Hub with Configurable I/O

2. Royalty-Free Driver Support

- Windows 11, 10, 8, 7 (Microsoft Certified WHQL Drivers)
- Windows Server 2008 R2, 2012, 2016, 2019, 2022
- Mac OS X
- Linux OS
- Android 3.2 and above

3. Ordering Information

Chip Product Name	Package Type	Ordering Part Number	MPQ
PL2561	32-pin QFN (5x5mm)	PL2561A2FRG8P1	2000pcs / reel

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4. Block Diagram

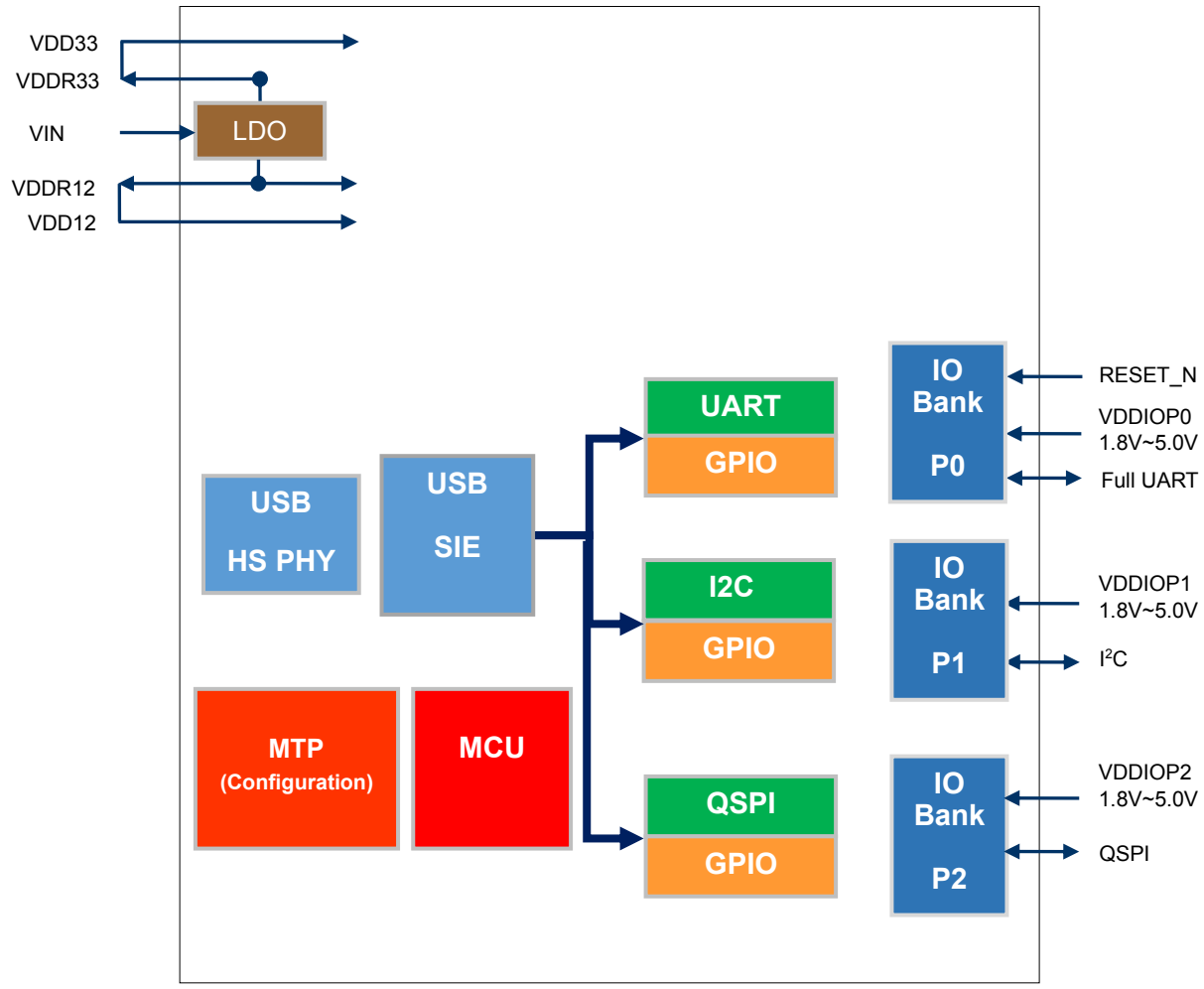

Figure 4-1: PL2561 **Block Diagram**

5. USB Logo Certification

TBD

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Table of Contents

1. Product Applications 5

2. Royalty-Free Driver Support.....5

3. Ordering Information 5

4. Block Diagram 6

5. USB Logo Certification 7

6. Overview 11

7. Pin Assignment & Description 12

7.1 PL2561 Pin Assignment 12

7.2 Pinout Description 13

7.3 GPIO Multi- Function Options..... 14

8. Functional description.....16

8.1 USB 2.0 HS Transceiver..... 16

8.2 LDO Regulator 16

8.3 USB HS/FS SIE..... 16

8.4 MCU..... 16

8.5 Internal MTPROM 16

8.6 UART Control 16

8.7 I^2C/SPI 17

8.8 IO Routing Logic..... 17

9. AC & DC Characteristics 18

9.1 Absolute Maximum Ratings 18

9.2 Operating Current..... 18

9.3 Recommended Operating Conditions..... 19

9.4 IO Characteristics..... 19

9.5 Timing parameters..... 22

9.6 Temperature Characteristics..... 22

9.7 Package Thermal Characteristics..... 23

9.8 Baud Rate Characteristics..... 23

9.9 SPI Frequency Characteristics 23

10. Package Outline Diagram 24

10.1 Outline Diagram (PKG CODE-WQFN)..... 24

11. Package information 25

11.1 Carrier Tape (QFN32) 25

11.2 Reel Dimension 25

List of Figures

Figure 4-1: PL2561 Block Diagram 6
Figure 7-1: PL2561 Pin Diagram 12
Figure 10-1: PL2561 Outline Diagram (QFN32 5x5mm、WQFN)..... 24

List of Tables

Table 7-1: USB Data Interface Pins..... 13
Table 7-2: Serial Interface Pins 13
Table 7-3: Configurable GPIO Pins..... 13
Table 7-4: Power and Ground Pins..... 14
Table 7-5: Miscellaneous Pins 14
Table 7-6: Configurable GPIO Multi-Function Pins..... 14
Table 7-7: GPIO Multi-Function Option Descriptions 15
Table 9-1: Absolute Maximum Ratings..... 18
Table 9-2: Operating Current Parameters 18
Table 9-3: Recommended Operating Conditions..... 19
Table 9-4: IO Characteristics at VDDIO=1.8V 19
Table 9-5: IO Characteristics at VDDIO=3.3V 20
Table 9-6: IO Characteristics at VDDIO=5.0V 21
Table 9-7: Timing parameters 22
Table 9-8 Temperature Characteristics 22
Table 9-9: Package Thermal Characteristics 23
Table 9-10 Baud Rate Characteristics 23
Table 9-11: SPI Frequency Characteristics..... 23

6. Overview

The new PL2561 chip provides multiple serial interfaces in a single-chip. Through USB HID class, there is no extra driver needs. The operating system or USB host communicates with the PL2561 through HID application software developed based on Windows/Mac/Linux DLL libraries provided by Prolific.

The PL2561 also integrates an USB 2.0 transceiver, Serial Interface Engine (SIE), LDO voltage regulator, power-on- reset (POR), FIFO data buffers, MTPROM and 9 GPIOs supported in 32 pin package except UART/I^{2}C/SPI function.

The PL2561 is designed for support UART/I^{2}C/SPI simultaneously. The BOM cost will be saved because it can support multiple function in one system by single chip.

The PL2561 added several new features and enhancements:

- No USB drivers needed through HID class.
- UART baud rate up to 115200 bps.
- SPI clock up to 32MHz.
- I^{2}C clock rate up to 1MHz.
- MTPROM can be programmed directly through USB (no high voltage generator required).
- Individual 512bytes FIFO for IN/OUT buffer per port.
- 9 configurable GPIO pins.
- Wide I/O voltage range (+1.8V ~ +5V) for port #0~2.
- Configurable I/O pin output driving strength.
- Unique USB Serial Number for each IC.

The PL2561 is available in 32-pin QFN package with Pb-free (RoHS compliant) green package.

7. Pin Assignment & Description

7.1 PL2561 Pin Assignment

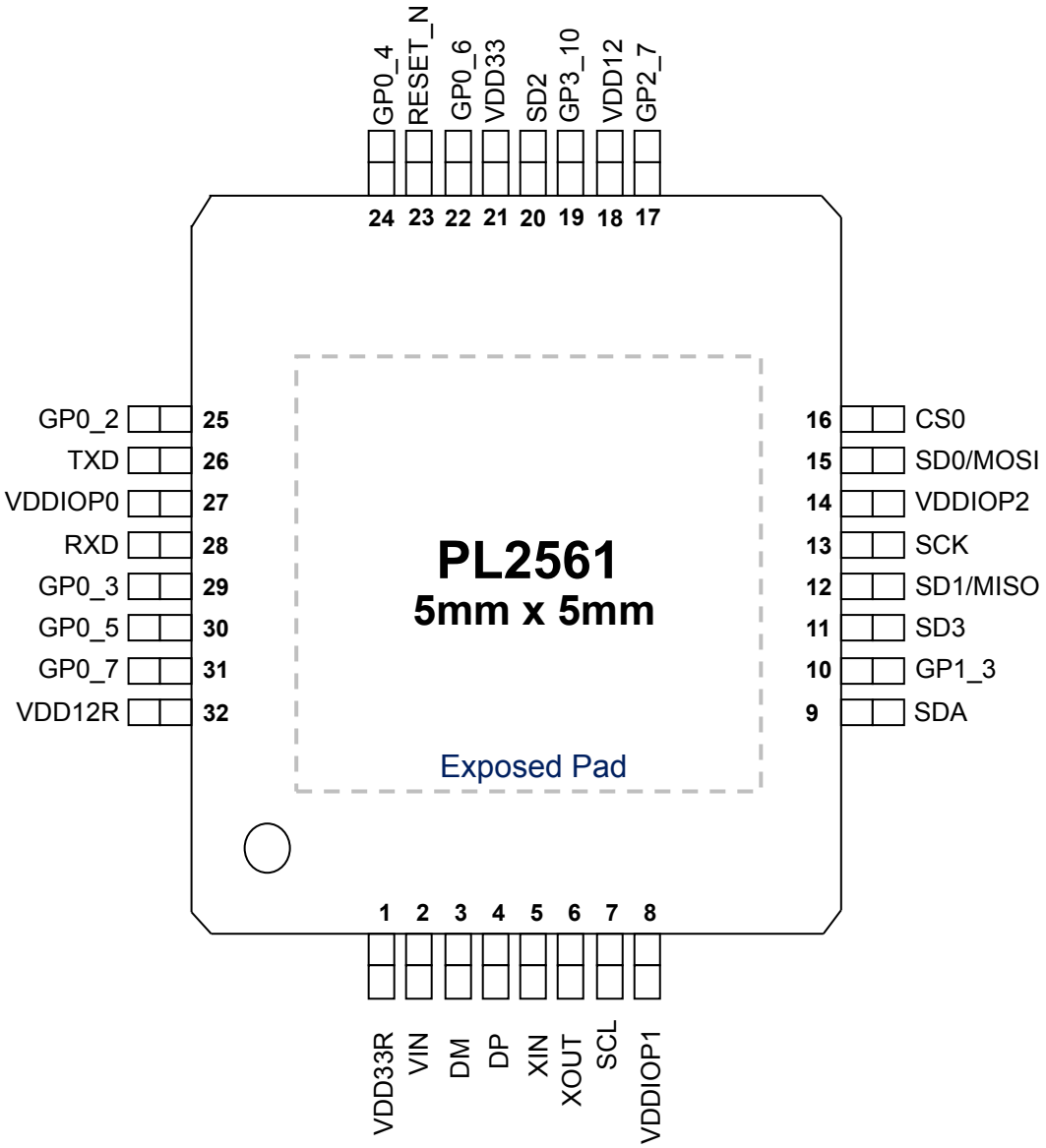


Figure 7-1: PL2561 Pin Diagram

7.2 Pinout Description

Table 7-1: USB Data Interface Pins

Pin Name	QFN32 Pin No.	Type	Description
DP	4	I/O	USB Port Data Plus (D+) Signal.
DM	3	I/O	USB Port Data Minus (D-) Signal.

Table 7-2: Serial Interface Pins

Pin Name	QFN32 Pin No.	Type	Description
TXD	26	Output	P0 Serial Port: Transmitted Data Output
RXD	28	Input	P0 Serial Port: Received Data Input
SCL	7	Output	I^2C port : Serial clock
SDA	9	I/O	I^2C port : Serial Data
SCK	13	Output	SPI(Serial Peripheral Interface) Port: Serial clock
SD0/MOSI	15	I/O	SPI Port: Serial data bit 0/ Master Output Slave Input
SD1/MISO	12	I/O	SPI Port: Serial data bit 1/ Master Input Slave Output
SD2	20	I/O	SPI Port: Serial data bit 2
SD3	11	I/O	SPI Port: Serial data bit 3
CS0	16	Output	SPI Port: chip select 0

NOTE: All input pins of UART function are default pull up

Table 7-3: Configurable GPIO Pins

Pin Name	QFN32 Pin No.	Type	Description
GP1_3	10	I/O	Configurable GPIO Pin. (see Section 7.3) **Factory default is GPIO input pin.**
GP2_7	17	I/O	Configurable GPIO Pin. (see Section 7.3) **Factory default is GPIO input pin.**
GP3_10	19	I/O	Configurable GPIO Pin. (see Section 7.3) **Factory default is GPIO input pin.**3 Note: Its I/O voltage is fixed at 3.3V and can't be changed with the external power.
GP0_6	22	I/O	Configurable GPIO Pin. (see Section 7.3) **Factory default is GPIO input pin.**
GP0_4	24	I/O	Configurable GPIO Pin. (see Section 7.3) **Factory default is GPIO input pin.**
GP0_2	25	I/O	Configurable GPIO Pin. (see Section 7.3) **Factory default is GPIO input pin.**
GP0_3	29	I/O	Configurable GPIO Pin. (see Section 7.3) **Factory default is GPIO input pin.**
GP0_5	30	I/O	Configurable GPIO Pin. (see Section 7.3) **Factory default is GPIO input pin.**
GP0_7	31	I/O	Configurable GPIO Pin. (see Section 7.3)

			Factory default is GPIO input pin. Note: The option of WAKEUP is also default enabled. It is used for the remote wakeup function that is to wake up chip from suspended state when this pin is toggled in suspend state.

NOTE: All GPIO pins are default Input mode.

Table 7-4: Power and Ground Pins

Pin Name	QFN32 Pin No.	Type	Description
VDDIOP0	27	Power	+1.8V to +5V P0 I/O signal power input pin. **Note: VDD_IO voltage should not larger than VIN voltage.**
VDDIOP1	8	Power	+1.8V to +5V P1 I/O signal power input pin.
VDDIOP2	14	Power	+1.8V to +5V P2 I/O signal power input pin.
VDD33	21	Power	+3.3V Power input
VDD33R	1	Power	+3.3V LDO regulator output.
VDD12R	32	Power	+1.2V LDO regulator output. **Note: Shall not be used for supplying external other circuits.**
VDD12	18	Power	+1.2V Power input and is connected to VDD12R internally.
VSS	33(Exposed Pad)	Power	Ground
VIN	2	Power	LDO regulator input. Supply power of +4.0V - +5.25V

Table 7-5: Miscellaneous Pins

Pin Name	QFN32 Pin No.	Type	Description
RESET_N	23	Input	Active low external reset pin input is used to reset the PL2561. NOTE: This pin is internal pulled high.
XI	5	Input	12MHz crystal oscillator input.
XOUT	6	Output	12MHz crystal oscillator output.

7.3 GPIO Multi- Function Options

The PL2561 chip (QFN32 package) provides a total of 9 configurable GPIO (General Purpose I/O) pins. The table below shows the possible functions that can be configured for each GPIO pin. These special functions can be easily configured in the MTPROM of the PL2561 using the Prolific MTPROM software tool. When these pins are configured as standard GPIO pins, customers can refer to the Prolific GPIO SDK (software development kit) to develop software to control the GPIO pins for desired functions in customer application.

Table 7-6: Configurable GPIO Multi-Function Pins

IO Pin	QFN32 Pin No.	Factory Default	Configurable Options (using MTP Tool)			
P0[2]	25	GPIO				
P0[3]	29	GPIO	PWMB			
P0[4]	24	GPIO	PWMA			
P0[5]	30	GPIO	PWMB			

P0[6]	22	GPIO	PWMA			
P0[7]	31	GPIO	CLK	BC_DET	WAKEUP	
P1[3]	10	GPIO	PWMB			
P2[7]	17	GPIO	CLK	VBUS_DET		
P3[10]	19	GPIO	SUSPEND_N			

Table 7-7: GPIO Multi-Function Option Descriptions

Function	QFN32 GPIO Pins	Type	Description
VBUS_DET	P2[7]	Input	When this pin is set to VBUS_DET mode, the device will not attach to USB until VBUS_DET input pin goes to high level. There must be only one pin configured as VBUS_DET pin. Refer above note for this special function.
BC_DET	P0[7]	Output	Battery Charge Detect pin. This active high pin indicates BC 1.2 DCP/CDP is detected.
SUSPEND_N	P3[10]	Output	Active low shutdown control pin during USB suspend. This pin is used to indicate chip entering suspend state when USB bus in idle state. Refer to above note for this special function.
WAKEUP	P0[7] (Pin 31)	Input	The remote wakeup function is to wake up chip from suspended state when this pin is toggled in suspend state.
CLK	P0[7] P2[7]	Output	Each channel has an independent clock output for external application. This pin can generate clock output up to 12MHz. Clock rates can be configured in MTPROM/EEPROM or customized driver.
PWMA	P0[4] P0[6]	Output	There are 2 independent PWMA and PWMB modules in the chip. Its max. frequency is about 7.6MHz. Users can refer to the programming guide in PL2561 SDK for details about how to enable PWM function and set its frequency and duty cycle.
PWMB	P0[3] P0[5] P1[3]	Output	There are 2 independent PWMA and PWMB modules in the chip. Its max. frequency is about 7.6MHz. Users can refer to the programming guide in PL2561 SDK for details about how to enable PWM function and set its frequency and duty cycle.

8. Functional description

8.1 USB 2.0 HS Transceiver

The USB Transceiver provides the USB high/full-speed electrical signal requirements and USB physical interface (DP/DM). This block includes the internal USB series termination resistors on the USB data lines and pull-up resistor for the DP signal. And the R_{REF} (resistor for reference power) also is included to save BOM cost.

8.2 LDO Regulator

This block is the 5V to 3.3V and 1.2V LDO regulator to power and drive the USB transceiver. It also includes 3.3V brownout detection output signals that will be used by digital circuit to reset the chip. The LDO 5V to 3.3V can supply 100mA for chip internal and external components.

8.3 USB HS/FS SIE

The USB High/Full-Speed Serial Interface Engine (SIE) block performs the processing of USB DP/DM signals. It translates the internal parallel data to serial data and outputs to USB HS/FS transceiver to generate external USB DP/DM signals timing. It also translates external USB DP/DM signals pass through USB HS/FS transceiver to parallel data for internal circuit. This block includes 15 IN/OUT endpoints. So there are sufficient multi interfaces supported by PL2561. Using these endpoints, it can implement multi functions in a single chip.

8.4 MCU

There is a MCU inside to handle USB standard requests and vendor requests. Many different configurations can be applied if different settings are configured in MTP. The MCU will depend on the value in MTP to do related setting for different implementation.

8.5 Internal MTPROM

The MTPROM (Multi-Time Programming Memory) is used as MCU firmware and chip function settings, GPIO pin function setting and USB descriptor related data. There is 768 bytes user programming area available for customization settings. This user programming area can be easily programmed by the Prolific MTPROM software through USB port without any additional voltage converter requirement.

8.6 UART Control

The UART Control module handles the data transfer according to UART format and interface. This module also includes a precise baud rate generator. Baud rate also supports wild range from 5 bps to 115200 bps and these baud rates setting are easily to set by popular terminal tool through USB command. So it can

support RS232, RS485 etc. The IO voltage level supports wild range from 1.8 to 5.0 V.

8.7 I²C/SPI

There are two more serial interfaces to control external devices for extend functions. They are SPI master control interface, I²C master/slave interface. I²C support fast/high speed mode for wide application. SPI master can support one/two/quad bit mode by configuration.

8.8 IO Routing Logic

The PL2561 has many versatile I/O functions. Each GPIO pin includes multiple functions that can be configured in the MTPROM. This module multiplexes I/O functions to different chip I/O pins. It also handles I/O pin polarity, open-drain, pull-up/pull-down, and I/O pin drive capability functions.

9. AC & DC Characteristics

9.1 Absolute Maximum Ratings

Table 9-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{VIN}	Power supply of VIN	-0.3 to 5.5	V
V_{DD12}	Power supply of VDD12	-0.3 to 1.3	V
V_{DD33}	Power supply of VDD33	-0.3 to 3.6	V
$V_{VDDIOP0}$	Power supply of VDDIOP0	+1.8 to V_{VIN}[1]	V
$V_{VDDIOP1}$	Power supply of VDDIOP1	+1.8 to V_{VIN}[1]	V
$V_{VDDIOP2}$	Power supply of VDDIOP2	+1.9 to V_{VIN}[1]	V
V_{INIOP0}	Input voltage of IO of P0	-0.3 to V_{VIN}[1]	V
V_{INIOP1}	Input voltage of IO of P1	-0.3 to V_{VIN}[1]	V
V_{INIOP2}	Input voltage of IO of P2	-0.3 to V_{VIN}[1]	V
V_{INIOP3}	Input voltage of IO of P3	-0.3 to +3.3V	V
V_{ESDHBM}	ESD HBM	6.0	KV
V_{ESDMM}	ESD MM	300	V
$I_{LATCHUP}$	Latch-up current	200	mA
T_{OP}	Operation temperature	-40 to 85	°C
T_{STG}	Storage temperature	-40 to 150	°C

1: shall not be higher than V_{VIN}

9.2 Operating Current

Table 9-2: Operating Current Parameters

Symbol	Parameter	Min	Typ	Max	Units
I_{VIN}	Current consumption of power supply. Testing condition → 1. bus power mode : power supply by USB VBUS 2. UART ports operate concurrently without LED/transceiver @ 115200 baud rate. 3 SPI flash /I^2C EEPROM power consumption is not included during accessing.		40		mA
I_{SUS}	Suspend current		900		uA

9.3 Recommended Operating Conditions

Table 9-3: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{VIN}	Power supply of VIN	4.0[2]		5.25	V
V_{DD12}	Power supply of VDD12	1.1	1.2	1.3	V
V_{DD33}	Power supply of VDD33	3.135		3.6	V
$V_{VDDIOP0}$	Power supply of VDDIOP0	1.8		V_{VIN}[1]	V
$V_{VDDIOP1}$	Power supply of VDDIOP1	1.8		V_{VIN} [1]	V
$V_{VDDIOP2}$	Power supply of VDDIOP2	1.9		V_{VIN} [1]	V
V_{INIOP0}	Input voltage of IO of P0	0		V_{VIN} [1]	V
V_{INIOP1}	Input voltage of IO of P1	0		V_{VIN} [1]	V
V_{INIOP2}	Input voltage of IO of P2	0		V_{VIN} [1]	V
V_{INIOP3}	Input voltage of IO of P3	0		3.3	V

1: shall not be higher than V_{VIN}

2: For using the internal 3.3V power from the internal 5-3.3V LDO

9.4 IO Characteristics

Table 9-4: IO Characteristics at VDDIO=1.8V

VIN=5.0V, VDD33=3.3V, VDD12=1.2V, **VDDIO=1.8V**, T=25 °C

Symbol		Parameter	Test Condition	Min	Typ	Max	Units
VIH		Input high voltage		1.8			V
VIL		Input low voltage				0.4	V
VOH		Output high voltage	IIO <= **IOH**	0.9*VDDIO			V
VOL		Output low voltage	IIO <= **IOL**			0.1*VDDIO	V
IOH	DRV=1	Driving high current	VIO >= 0.9*VDDIO			1.8	mA
	DRV=2	Driving high current	VIO >= 0.9*VDDIO			2.1	mA
	DRV=3	Driving high current	VIO >= 0.9*VDDIO			2.3	mA
IOL	DRV=1	Driving low current	VIO <= 0.1*VDDIO			20	mA
	DRV=2	Driving low current	VIO <= 0.1*VDDIO			22	mA
	DRV=3	Driving low current	VIO <= 0.1*VDDIO			24	mA
T_{RISE}	DRV=1	Rise time	20pF loading, 10% to 90%		28		ns
	DRV=2	Rise time	20pF loading, 10% to 90%		25		ns
	DRV=3	Rise time	20pF loading, 10% to 90%		23		ns
T_{FALL}	DRV=1	Fall time	20pF loading, 90% to 10%		0.7		ns
	DRV=2	Fall time	20pF loading, 90% to 10%		0.6		ns
	DRV=3	Fall time	20pF loading, 90% to 10%		0.5		ns

FBAUD	DRV=1	UART baud rate				115200	bps
	DRV=2	UART baud rate				115200	bps
	DRV=3	UART baud rate				115200	bps
RPULLUP		Pull-up resistance			75.6K		Ohm
RPULLDOWN		Pull-down resistance			72K		Ohm
ILEAKHI		Input high leakage	VIO = VDDIO Pull-up/pull-down disabled		23		uA
ILEAKLO		Input low leakage	VIO = 0V Pull-up/pull-down disabled		23		uA

Table 9-5: IO Characteristics at VDDIO=3.3V

VIN=5.0V, VDD33=3.3V, VDD12=1.2V, **VDDIO=3.3V**, T=25 °C

Symbol		Parameter	Test Condition	Min	Typ	Max	Units
VIH		Input high voltage		TBM			V
VIL		Input low voltage				TBM	V
VOH		Output high voltage	IIO <= **IOH**	0.9*VDDIO			V
VOL		Output low voltage	IIO <= **IOL**			0.1*VDDIO	V
IOH	DRV=1	Driving high current	VIO >= 0.9*VDDIO			11	mA
	DRV=2	Driving high current	VIO >= 0.9*VDDIO			17	mA
	DRV=3	Driving high current	VIO >= 0.9*VDDIO			22	mA
IOL	DRV=1	Driving low current	VIO <= 0.1*VDDIO			12	mA
	DRV=2	Driving low current	VIO <= 0.1*VDDIO			18	mA
	DRV=3	Driving low current	VIO <= 0.1*VDDIO			24	mA
TRISE	DRV=1	Rise time	10pF loading, 10% to 90%		4		ns
	DRV=2	Rise time	10pF loading, 10% to 90%		2		ns
	DRV=3	Rise time	10pF loading, 10% to 90%		2		ns
TFALL	DRV=1	Fall time	10pF loading, 90% to 10%		1		ns
	DRV=2	Fall time	10pF loading, 90% to 10%		1		ns
	DRV=3	Fall time	10pF loading, 90% to 10%		1		ns
FBAUD	DRV=1	UART baud rate				115200	bps
	DRV=2	UART baud rate				115200	bps
	DRV=3	UART baud rate				115200	bps
RPULLUP		Pull-up resistance			75.6K		Ohm
RPULLDOWN		Pull-down resistance			72K		Ohm
ILEAKHI		Input high leakage	VIO = VDDIO		43		uA

			Pull-up/pull-down disabled				
ILEAKLO		Input low leakage	VIO = 0V Pull-up/pull-down disabled		43		uA

Table 9-6: IO Characteristics at VDDIO=5.0V

VIN=5.0V, VDD33=3.3V, VDD12=1.2V, **VDDIO=5.0V**, T=25 °C

Symbol		Parameter	Test Condition	Min	Typ	Max	Units
VIH		Input high voltage		TBM			V
VIL		Input low voltage				TBM	V
VOH		Output high voltage	IIO <= **IOH**	0.9*VDDIO			V
VOL		Output low voltage	IIO <= **IOL**			0.1*VDDIO	V
IOH	DRV=1	Driving high current	VIO >= 0.9*VDDIO			20	mA
	DRV=2	Driving high current	VIO >= 0.9*VDDIO			28	mA
	DRV=3	Driving high current	VIO >= 0.9*VDDIO			38	mA
IOL	DRV=1	Driving low current	VIO <= 0.1*VDDIO			20	mA
	DRV=2	Driving low current	VIO <= 0.1*VDDIO			28	mA
	DRV=3	Driving low current	VIO <= 0.1*VDDIO			36	mA
TRISE	DRV=1	Rise time	20pF loading, 10% to 90%		2		ns
	DRV=2	Rise time	20pF loading, 10% to 90%		2		ns
	DRV=3	Rise time	20pF loading, 10% to 90%		1.5		ns
TFALL	DRV=1	Fall time	20pF loading, 90% to 10%		1.5		ns
	DRV=2	Fall time	20pF loading, 90% to 10%		1.5		ns
	DRV=3	Fall time	20pF loading, 90% to 10%		1.5		ns
FBAUD	DRV=1	UART baud rate				115200	bps
	DRV=2	UART baud rate				115200	bps
	DRV=3	UART baud rate				115200	bps
RPULLUP		Pull-up resistance			75.6K		Ohm
RPULLDOWN		Pull-down resistance			72K		Ohm
ILEAKHI		Input high leakage	VIO = VDDIO Pull-up/pull-down disabled		65		uA
ILEAKLO		Input low leakage	VIO = 0V Pull-up/pull-down disabled		65		uA

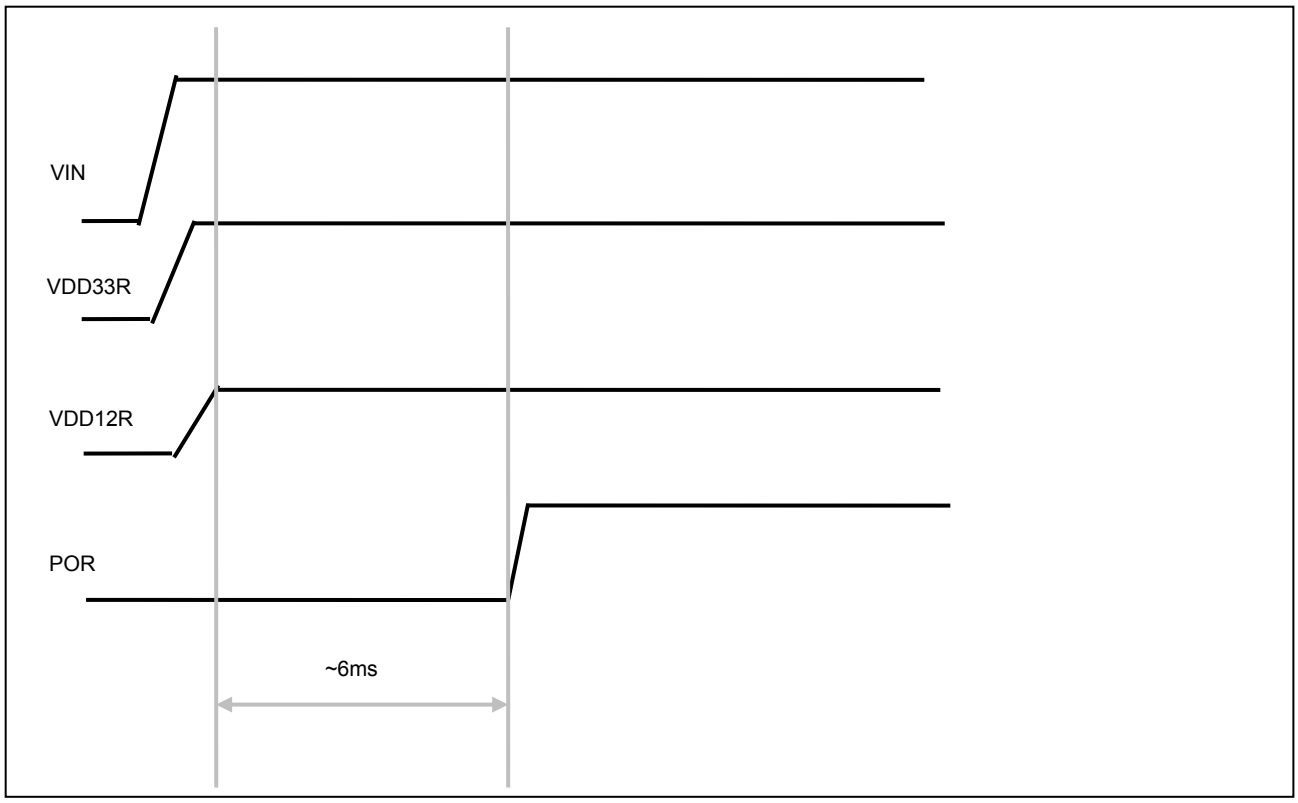
9.5 Timing parameters

Table 9-7: Timing parameters

Symbol	Parameter	Min	Typ	Max	Units
T_{POR}			6		ms

Chip Reset Control

The PL2561 has an internal power on reset circuit; therefore, external reset control circuit is optional. External reset control (RESET_N pin) can help system designs to make sure of chip operation start time.



9.6 Temperature Characteristics

Table 9-8 Temperature Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature (ambient)	--	-40	--	85	°C
Junction Operation Temperature	T_J	-40	25	125	°C

9.7 Package Thermal Characteristics

Table 9-9: Package Thermal Characteristics

SYMBOL	PARAMETER	RATING	UNITS
θ ja	Junction-to-ambient thermal resistance	29	℃/W
θ jc	Junction-to-case thermal resistance	15	℃/W

9.8 Baud Rate Characteristics

Table 9-10 Baud Rate Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Baud rate @ VDD_IO = 5V	--	5	--	115200	bps
Baud rate @ VDD_IO = 3.3V	--	5	--	115200	bps
Baud rate @ VDD_IO = 1.8V	--	5	--	115200	bps

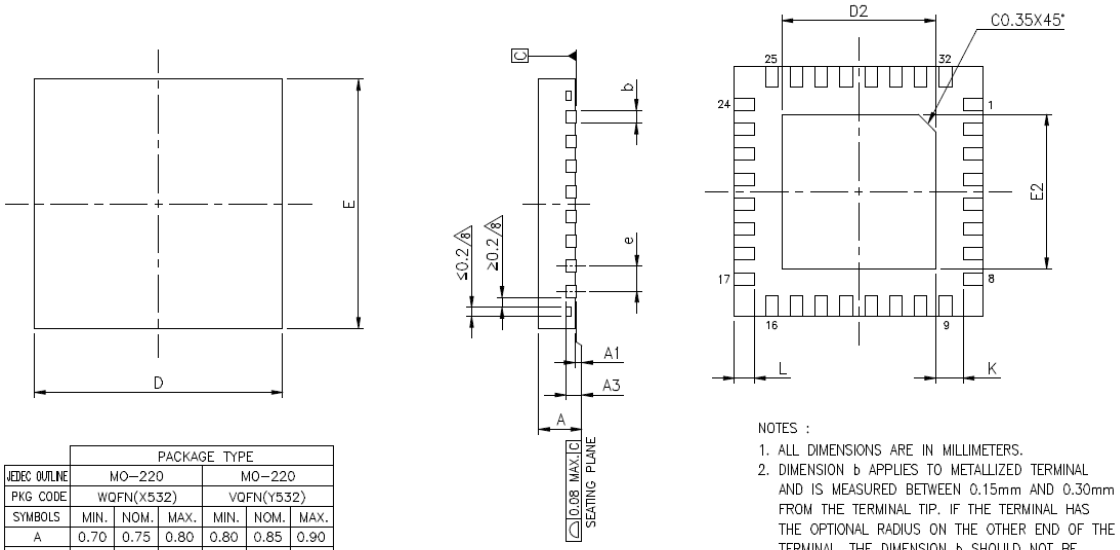
9.9 SPI Frequency Characteristics

Table 9-11: SPI Frequency Characteristics

Parameter	Test Condition	Min	Typ	Max	Units
SPI Freq. @ VDDIOP2 = **1.9V**	-SPI NOR flash: GD25WQ128E -Power supply of VCC of SPI flash: 2.0V - Operating Temperature: -40 and 85 ºC			32	MHz

10. Package Outline Diagram

10.1 Outline Diagram (PKG CODE-WQFN)



	PACKAGE TYPE					
JEDEC OUTLINE	MO-220			MO-220		
PKG CODE	WQFN(X532)			VQFN(Y532)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.203 REF.			0.203 REF.		
b	0.18	0.25	0.30	0.18	0.25	0.30
D	5.00 BSC			5.00 BSC		
E	5.00 BSC			5.00 BSC		
e	0.50 BSC			0.50 BSC		
L	0.35	0.40	0.45	0.35	0.40	0.45
K	0.20	—	—	0.20	—	—

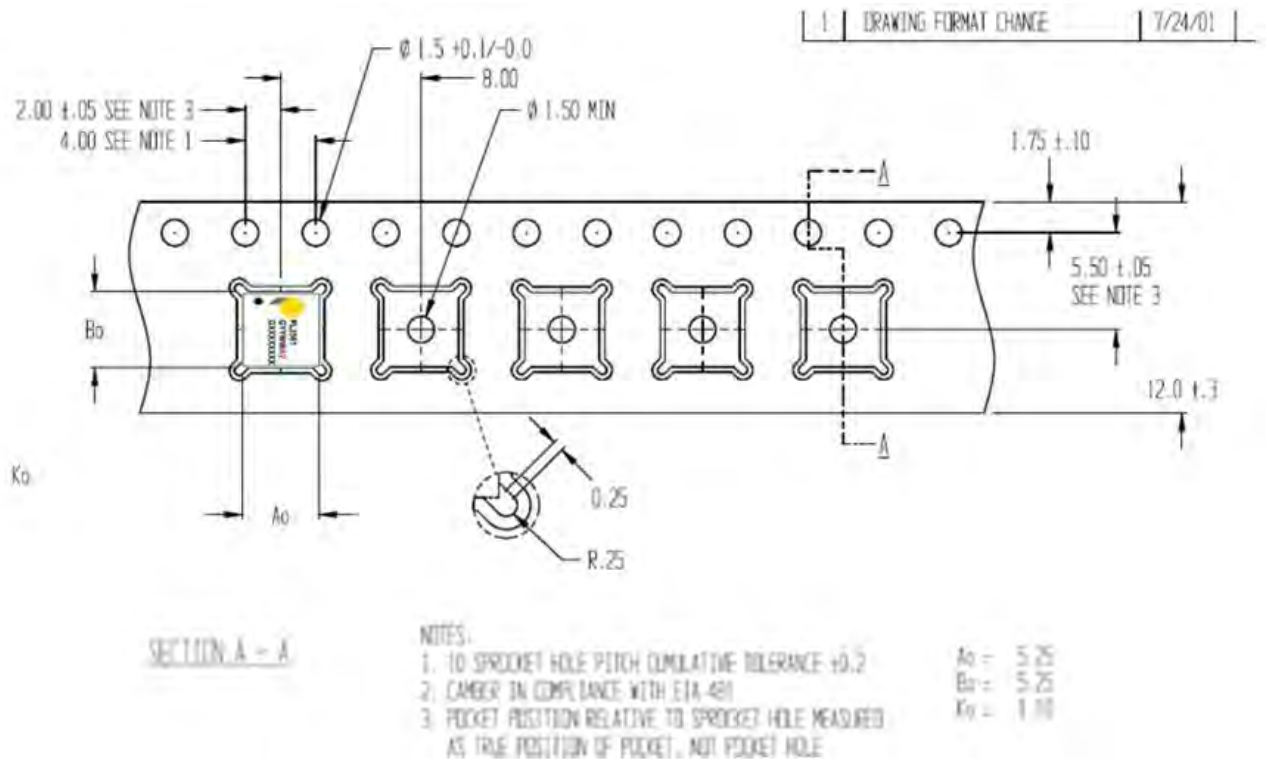
	E2			D2			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
153X153 MIL	3.15	3.25	3.30	3.15	3.25	3.30	V	V	W(V)HHD-5

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

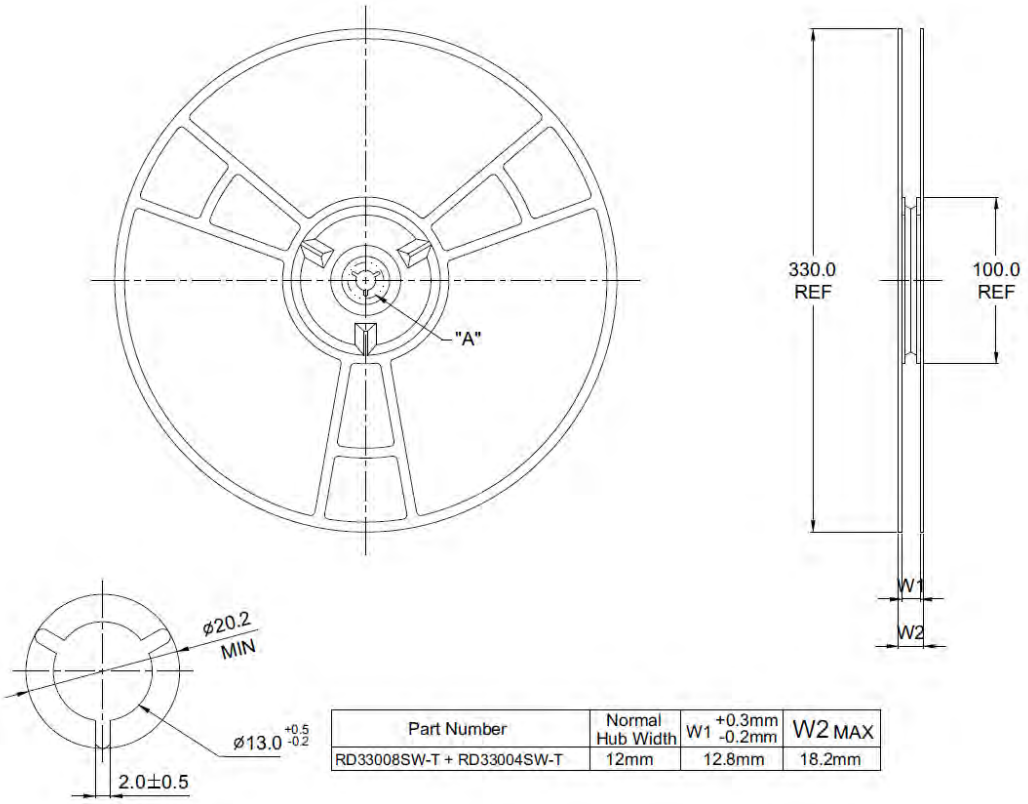
Figure 10-1: PL2561 Outline Diagram (QFN32 5x5mm、WQFN)

11. Package information

11.1 Carrier Tape (QFN32)



11.2 Reel Dimension



Part Number	Normal Hub Width	W1 +0.3mm -0.2mm	W2 MAX
RD33008SW-T + RD33004SW-T	12mm	12.8mm	18.2mm

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