PL2732

USB 3.0 eMMC Storage Controller

PCB Layout Guidelines

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Prolific Technology Inc.
7F, No. 48, Sec. 3, Nan Kang Rd.
Nan Kang, Taipei 115, Taiwan, R.O.C.
Telephone: +886-2-2654-6363
Fax: +886-2-2654-6161
E-mail: sales@prolific.com.tw
Website: http://www.prolific.com.tw

Table of Contents

Overview

The guidelines provide the recommended consideration on PCB layout.

1. USB3.0 trace

- USB3.0 signal traces consists of two differential pair traces, a transmit pair (SSTX+ and SSTX-) and a receive pair (SSRX+ and SSRX-). Each differential pair traces should be routed with differential impedance of 90±7 ohms.

- Never route USB3.0 differential traces near other high frequency traces such as the signal traces of USB2.0, eMMC and crystal to avoid crosstalk.

  Ways to Avoid Crosstalk:

  -Use the 3W rule (3 times the width of USB3.0 signal trace as figure 1) to separate USB3.0 signal trace from other high frequency traces.

  -Use ground traces/guards around either USB3.0 signal or other high frequency signal traces.

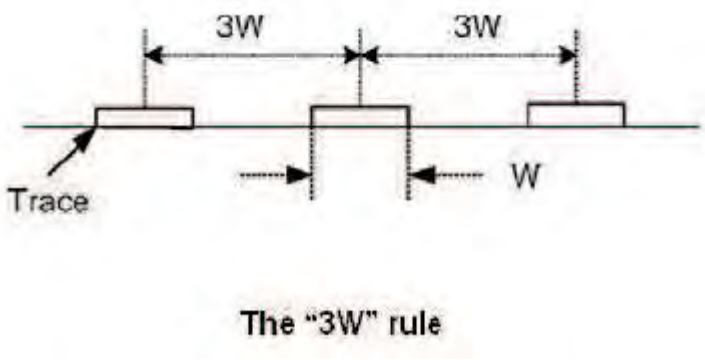

Figure 1

- Never route USB3.0 differential traces near the PCB edge to prevent from the distortion of USB3.0 signal by EMI and ESD.

- Never route USB3.0 differential traces over the split ground and power planes as figure 2. For a worse example as Figure 2, USB3.0 differential pair is routed on the top layer of PCB and overlapped a split ground plane with other signal traces on the second layer(for 4-layer PCB) or the bottom layer(for 2-layer PCB) of PCB.

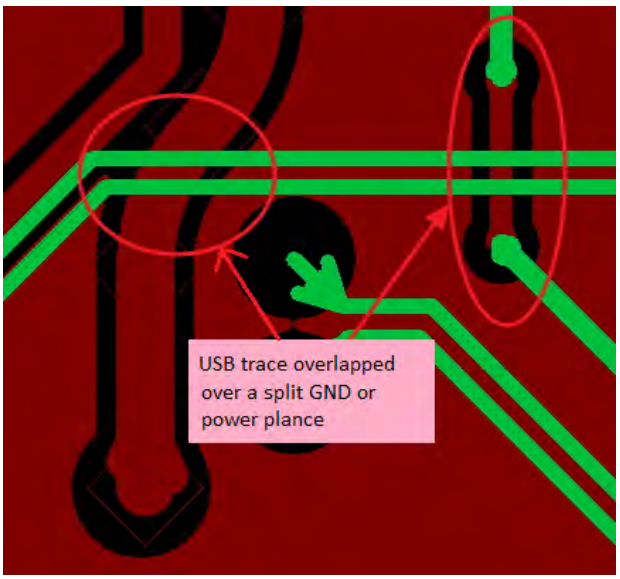

Figure 2

- It is allowed to swap the plus and minus traces of USB3.0 signal SSTX and SSRX. This can prevent one of the differential traces from crossing over one another. However, it is not permissible to swap the transmitter differential pair (SSTX signal) with the receiver differential pair (SSRX signal).

- The length of one trace of each differential pair should be as the same as possible with another trace. Maximum trace length mismatch between USB3.0 signal pairs should be no greater than 100 mils.

- When using a common mode choke and an ESD protect part to suppress EMI and ESD, they should be placed as close as possible to the USB3.0 connector.

- The transmitter differential pair requires two 0.1 µF coupling capacitors for proper operation. The package size of these capacitors should be no bigger than 0603 and placed symmetrically as close as possible to signal pins of USB3.0 connector.

- It is recommended to straight route USB3.0 differential pair and less route them with bends as figure 3.

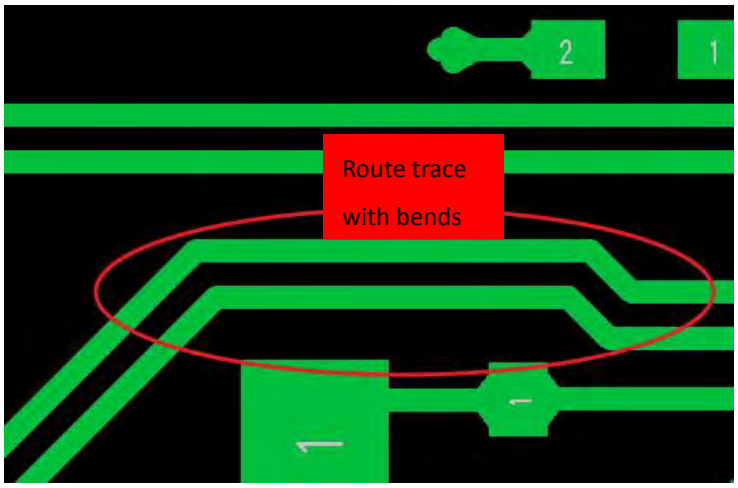

Figure 3

2. USB2.0 trace

- USB2.0 differential pair traces should be routed with differential impedance of 90±15% ohms.
- The trace length of one trace of USB2.0 differential pair should be as the same as possible with another trace. Maximum trace length mismatch between USB signal pairs should be no greater than 100 mils.
- When using a common mode choke and an ESD protect part to suppress EMI and ESD, they should be placed as close as possible to the USB connector.
- Never route USB2.0 differential traces over the split ground and power planes on the different and adjacent layer of PCB.

3. Power

- Place decoupling capacitors near the power pin of PL2732.
- Minimum trace width of VBUS of USB connector is 20 mils.
- Minimum trace width of 1.2V, 3.3V and eMMC power is 13 mils.

4. Others

- Pin VBUSDET0 (pin 32) of PL2732 is an I/O pin and used for detecting the connection of USB host controller with USB VBUS voltage. Not apply the power trace width for it.
- NC pins of 4-pin crystal should be connected to GND to prevent from generating EMI.
- The eMMC signal traces should be length matched. Maximum trace length mismatch should be no greater than 100 mils.

- Never route eMMC signal traces near other high frequency traces such as the signal traces of USB and crystal to avoid crosstalk.

  Ways to Avoid Crosstalk:

  -Use the 3W rule (3 times the width of eMMC signal trace) to separate eMMC signal trace from other high frequency traces.

  -Use ground traces/guards around either eMMC signal or other high frequency signal traces.

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