4-Channel Power/Energy Metering Analog Front End (AFE)

Product Datasheet PL7413

Features

- 4-Channel 24-bit sigma-delta ADC
- Internal 3.3V to 1.8V cap-less LDO
- Internal 1.2V cap-less VREF (w/ 0.1% accuracy/full temp. range after trim)
- Built-in 1X ~ 32X PGA (w/ 0.1% accuracy/full temp. range after calibration)
- Internal 16MHz RC OSC (w/ 0.2% accuracy/full temp. range after trim)
- Internal VDT/POR and temperature sensor
- Built-in FIR filter for each individual channel
- Channel phase alignment
- Programmable 48-bit DSP engine with
  - 512 x 32 program space
  - 128 x 48 data space
  - 64 x 48 output buffer
  - Built-in fix point to float-point converter
- 8KB OTP with 2 banks DSP code, DSP CFG and SYS CFG
- Supports I2C/SPI/UART (UART supports auto baud-rate mode)
- Supports 38KHz IR carrier removed
- Supports up to 9 GPIOs which can be directly controlled by DSP
- Small package size: 4x4 QFN24

Typical Applications

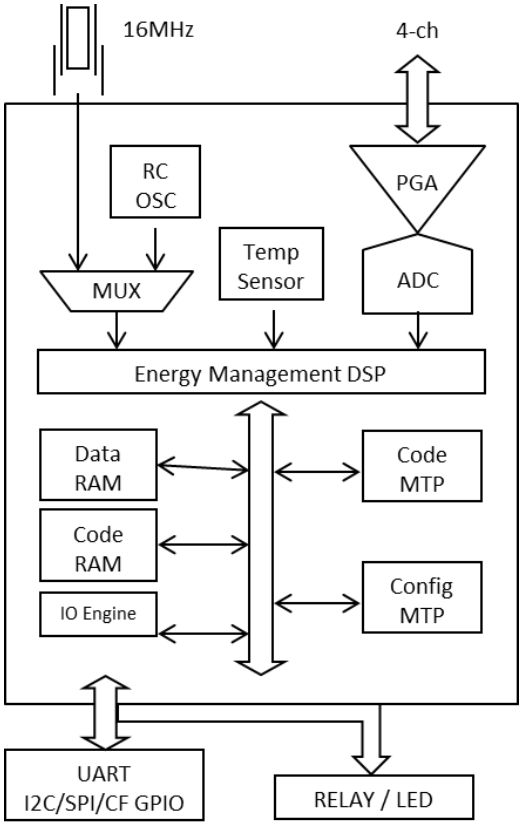
- Smart Plug/Strip/PDU
- Protection Device/Home Appliance
- Power Monitor, Hardware Monitor

General Description

The PL7413 is a highly integrated power/energy monitoring Analog Front End (AFE) IC that measures electricity-related data for power usage measurement applications. It has built-in 8-channel ADC and a programmable DSP which can adapt to different applications such as metering, power protection and Master/Slave.

The PL7413 has a built-in MTP that stores the chip configuration, DSP code and calibration data. It provides SPI slave interface and can be used for calibration and programming data or DSP code. MCU can be accessed through SPI interface.

The PL7413 can diagnose the electricity-related data to identify overloading, short circuit, leakage current and arcing condition for further power protection features. It also provides a flexible architecture, low system BOM cost and programmable solution, to help manufacturers minimize development efforts and design a versatile and flexible product.



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Block Diagram

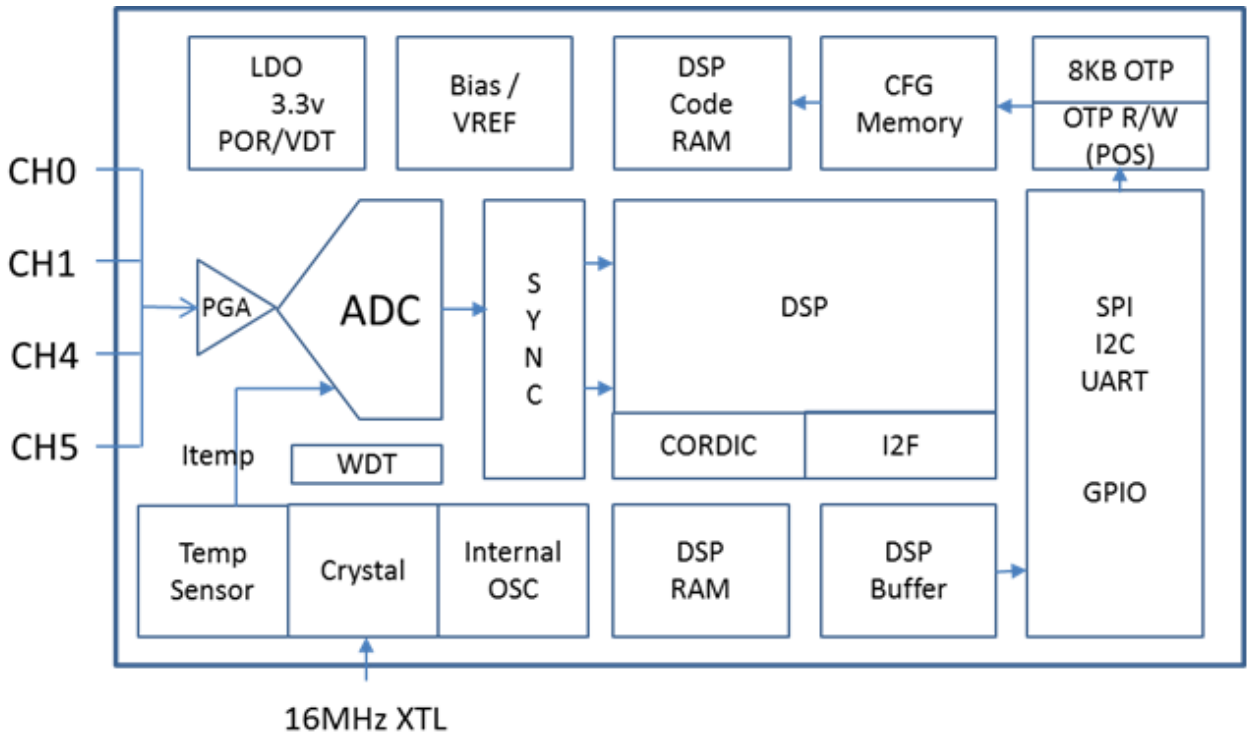

Figure 1-1: Function Block Diagram

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1. Detailed Features

1.1 General Features

- 4-Channel 24-bit sigma-delta ADC
- H/W DSP for power parameter calculation
- DSP Code upgradeable by MCU
- Low power consumption
  - 4.6mA@3.3V, full operation
  - 2.3mA@3.3V, low power mode
- Operation temperature range: -20 ^{o}C to +85 ^{o}C
- Small package size: 4x4 QFN24

1.2 ADC

- 24-bit ADC with PGA
- PGA Gain 1X ~ 32X
- 4-Channel individual decimator
- 3-Channel differential and 1-Channel single-end input
- Built-in internal 1.2V VREF for ADC measurement
- VREF accuracy is +/- 0.2%
- Channel data phase aligner
- Built-in FIR filter for each channel

1.3 DSP

- Programmable 48-bit DSP engine with
  - 512 x 32 program space
  - 128 x 48 data space
  - 64 x 48 output buffer
- 8KB OTP with 2 banks DSP code, DSP CFG and SYS CFG
- Supports RMS, active power, reactive power, apparent power, Power factor, KWH calculation
- SAG/SWELL, Over-Current, Over-Watt, Leakage Protection
- THD/Harmonic Calculation
- Supports AC/DC measurement (possible to dynamic adjust by MCU)
- Built-in fix-point to IEEE 754 floating point format converter

1.4 Clock System

- Supports up to 16MHz external crystal input
- Built-in internal 16MHz +/- 5% OSC
- Anti-fail clock auto switch
- System clock divider for each block
- Built-in internal watch-dog timer with IO interrupt output

1.5 SPI Interface

- SPI Slave mode supports mode 0, mode 1, mode 2, and mode 3
- Supports single and multi-byte read/write
- Supports CRC data check

1.6 I2C Interface

- I2C interface
- Two hardware slave ID selection for cascade application
- Software ID programmable
- Supports single and multi-byte read/write
- Supports CRC data check

1.7 UART

- Auto baud-rate learning
- Two hardware slave ID selection for cascade application
- Software ID programmable
- Supports single and multi-byte read/write
- Supports CRC data check
- Supports UART timeout
- Supports IR 38KHz carrier removed
- UART master mode for auto data report

1.8 GPIO

- Programmable IN/OUT control
- Selectable control by DSP or register setting

2. Pin Out Diagram and Description

2.1 24-Pin QFN Pin Diagram

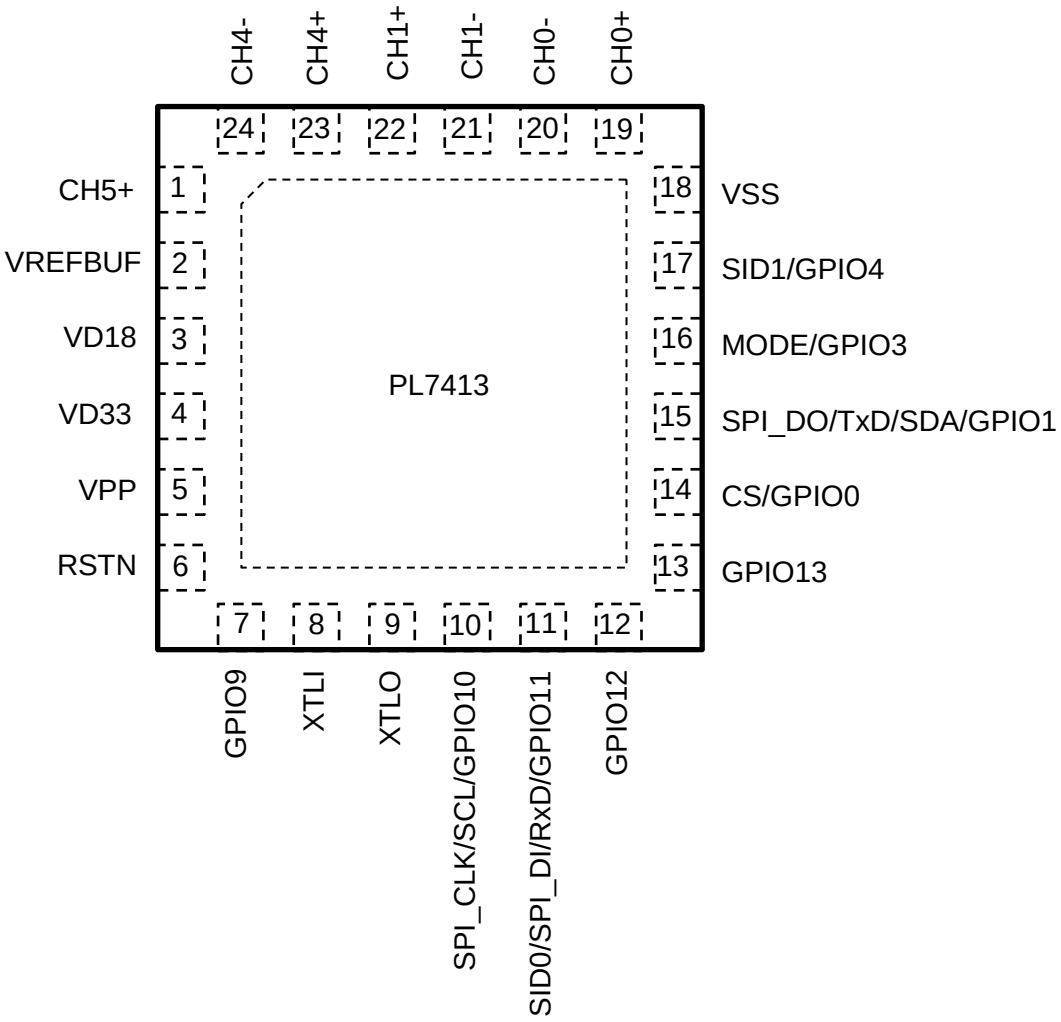


Figure 2-1: PL7413 Pin Diagram (QFN24)

2.2 24-Pin QFN Pin-Out Description

Table 2-1：PL7413 QFN24 Pin Name Table

Pin #	Pin Name	Type	Pin Description
1	CH5	Analog Input	Analog CH5 differential input
2	VREFBUF	Analog Output	The reference value is 1.2V.
3	VD18	Power	1.8V LDO output (Analog)
4	VD33	Power	VDD33 output
5	VPP	Power	OTP 6.5V programming power input
6	RSTN	Digital Input/Output	Reset input (active low)
7	GPIO9	Digital Input/Output	GPIO#9
8	XTLI	Crystal Input	16MHz Crystal input pad
9	XTLO	Crystal Output	16MHz Crystal output pad
10	SP_CLK/SCL/GPIO10	Digital Input/Output	Multi-function IO, GPIO#10
11	SID0/SPI_DI/RxD/ GPIO11	Digital Input/Output	Multi-function IO, GPIO#11
12	GPIO12	Digital Input/Output	GPIO#12
13	GPIO13	Digital Input/Output	GPIO#13
14	CS/GPIO0	Digital Input/Output	Multi-function IO, GPIO#0
15	SPI_DO/TxD/SDA/GPIO1	Digital Input/Output	Multi-function IO, GPIO#1
16	MODE/GPIO3	Digital Input/Output	Multi-function IO, GPIO#3
17	SID1/GPIO4	Digital Input/Output	Multi-function IO, GPIO#4
18	VSS	Ground	Digital Ground
19	CH0+	Analog Input	Analog CH0 differential input +
20	CH0-	Analog Input	Analog CH0 differential input -
21	CH1-	Analog Input	Analog CH1 differential input -
22	CH1+	Analog Input	Analog CH1 differential input +
23	CH4+	Analog Input	Analog CH4 differential input +
24	CH4-	Analog Input	Analog CH4 differential input -

3. Electrical Characteristic

3.1 Absolute Maximum Rating

Table 3-1：Absolute Maximum Rating

Parameter	Max Value
AVDD3	4.0V
DVDD3	4.0V
Analog input	-0.5V ~ +0.5V
Digital I/O input	-0.3V ~ AVDD + 0.3V
Input Current (Digital IO)	20uA
Output Current (IO Pin)	6mA
Operation Temperature	-20°C ~ 85°C
Storage Temperature	-40°C ~ 150°C
ESD	4KV(HBM)/500V(MM)

3.2 Recommended Operation Conditions

Table 3-2：Recommended Operation Conditions

Parameter	Max Value
AVDD3	3.0V ~ 3.3V
DVDD3	3.0V ~ 3.3V
VPP	6.5
Analog input	-0.3V ~ 0.3V
XTL	16MHz

3.3 AC/DC Characteristics

Table 3-3：AC/DC Characteristics

(All parameters apply at VDD=3.3 V±10%, AGND=DGND=0 V, Internal Reference, XTAL=8MHz, TMIN to TMAX = - 20°C to +85°C.)

Parameters	Test Condition	Min.	Typ.	Max.	Units
VAIN	ADC input (differential)	-0.45		0.45	V
	ADC Single-end w buffer	0.2		0.9	V
	ADC Single-end wo buffer	-0.45		0.45	V
PGA	Gain 1X, 2X, 4X, 8X, 16X, 32X				
VADC	PGA=1X	-320		320	mV
	PGA=2X	-160		160	mV
	PGA=4X	-80		80	mV
	PGA=8X	-40		40	mV
	PGA=16X	-20		20	mV

	PGA=32X	-10		10	mV
ADC	Data output		24		Bits
	Data range	-2^22		2^22	
	OSR selection: 64/128/256				
	Latency selection	4		7	
	ADC noise free bits		14.5		Bits
ODR	ADC output data rate (depends on channel mux setting)			1600	SPS
OSC					
Fosc	Internal OSC frequency		16		MHz
Icc_osc					uA
	Trimming step		20		KHz
	Internal OSC stability (-20~85C)				%
XTL PAD			16		MHz
	Duty cycle		50		%
	Crystal start-up time				us
IO PAD					
VIH		2.3			V
VIL				1	V
VOH		3.0			V
VOL				0.3	V
	I2C speed@16MHz		400		KHz
	SPI speed@16MHz		2		MHz
	UART baud rate@16MHz		115		KHz
Power Consumption					
Icc	2 LED / 2 ambient 200 samples second				mA
	2 LED / 2 ambient 100 samples second				mA
	2 LED / 2 ambient 50 samples second				mA

4. Function Description

4.1 AFE (Analog Front-End)

The PL7413 can work as an AFE (Analog Front-End) with SPI interface. It can measure the V/I real-time data, V/I rms, Watt, VA, PF, and line frequency. Users can utilize this information for further energy management. The following table depicts the parameters that can be accessed through the PL7413 SPI interface.

Table 4-1：AFE Measurement Parameters

Parameter	Description
V_{RMS}	RMS value of voltage
I_{RMS}	RMS value of current
Power	Active power value
PF	Power Factor
Frequency	Line Frequency

4.2 Power Protection

The power protection function of PL7413 prevents overload condition that may cause equipment to overheat or catch fire. When the load current exceeds the rated current (or pre-configured current threshold, $I_{LT/ST}$) for a specified time, the relay will be switched off to prevent overheat condition. Both the overload threshold current and delay time to switch off relay can be configured through the software provided by Prolific.

4.2.1 Power Protection Operation

The power protection operation is shown in Figure 4-1 and Figure 4-2:

- If the load current (I_{LOAD}) is less than or equal to $I_{LT/ST}$, the relay is always ON.
- If the load current (I_{LOAD}) is larger than $I_{LT/ST}$, the delay time (T_{OFF}) to switch off relay will be shorter. Refer to section 4.2.2 to calculate (T_{OFF}).
- Both the $I_{LT/ST}$ and $T_{LT/ST}$ can be configured by the application software provided by Prolific.

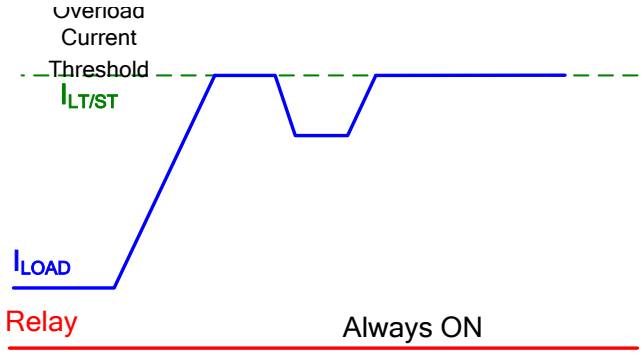


Figure 4-1: Description of long/short time protection (I_{LOAD} = $I_{LS/ST}$)

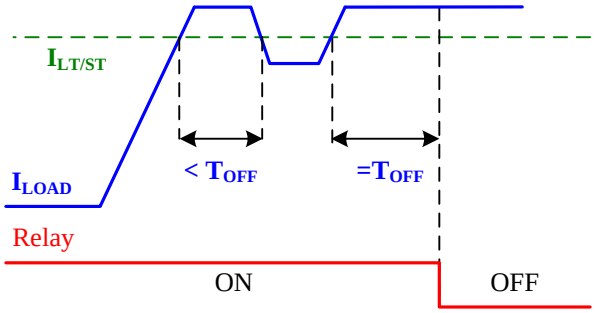


Figure 4-2: Description of long/short time protection (I_{LOAD} > $I_{LS/ST}$)

4.2.2 Delay Time to switch off relay

The delay time, T_{OFF}, can be calculated by the following equation:

$$T_{OFF} = T_{LT/ST} \times \left(\frac{I_{LT/ST}}{I_{LOAD}} \right)^2$$

For example,

- Short time threshold current (I_{ST}) is set as 30A
- T_{ST} is set as 5sec
- Exact load current is 50A.

The delay time to switch off relay is:

$$T_{OFF} = 5 \times \left(30 / 50 \right)^2 = 1.8 \text{sec}$$

5. Interface

- **IO Mode Selection**

  IO Mode is latched when resetn is from low to high.

  - i2c_en = [MODE pin, CS pin]= 2'b00
  - uart_en = [MODE pin, CS pin]= 2'b01
  - spi_en = [MODE pin, CS pin]= 2'b10
  - gpio_en = [MODE pin, CS pin]= 2'b11

5.1 SPI Interface

The SPI bus is the interface to access internal memory/register/energy information of PL7413. The SPI interface of PL7413 is operated at slave mode; consequently, the external SPI device should serve as the SPI master. As shown in below diagram, the external SPI master sends Chip Select and Clock signal to SPI slave of PL7413. Data is written through SPI_DI and read through SPI_DO.

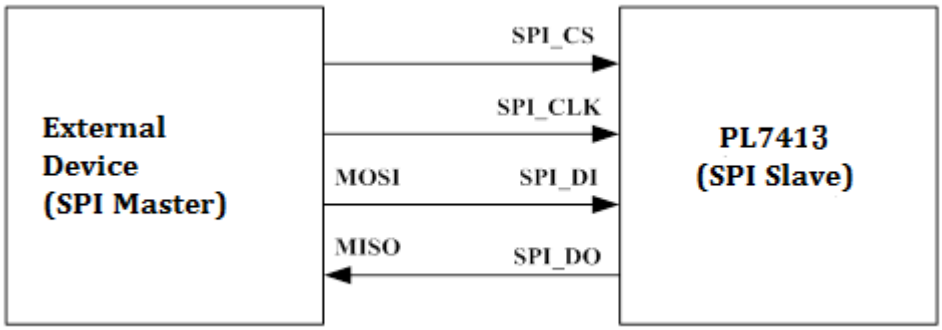


Figure 5-1: Connection scheme of SPI interface

5.1.1 SPI Command

- **spi_cmd[7]:** inc_adr_dis 1: disable address increment

  Ex: checking whether dsp is ready. The address can be fixed.

  dsp_status(cfg addr = 0x390a).

  If DSPRDY is from 0 to 1, then master can read out dsp outbuffer data.

- **spi_cmd[6:4]:** read/write command
  - spi_cmd[6:4] = 3'h1 for read with crc enable
  - spi_cmd[6:4] = 3'h2 for write with crc enable
  - spi_cmd[6:4] = 3'h3 for read with crc disable
  - spi_cmd[6:4] = 3'h4 for write with crc disable
- **spi_cmd[3:0]:** Read/Write package number

- case1: crc enable, set to 4, master must send out 4byte data + 1byte crc. Then slave will send out internal crc value to master.
- case2: crc disable, set to 4, master must send out 4byte data. Then slave will not send out internal crc value to master.

5.1.2 SPI Mode

Default SPI is at mode3 and can be changed at power on sequence (OTP value).

➢ *spi_con = 0x3837(Must write the setting in OTP-CFG Bank0 at the start).*

- Bit7 = cpol, clock polarity
- Bit6 = cpha, clock phase
- Bit5 = spr1, to select spi master clk
- Bit4 = spr0, to select spi master clk
- Bit3~0: no use
- SPI master clk = fclk/2 (00), fclk/4(01), fclk/8(10), fclk/16(11)

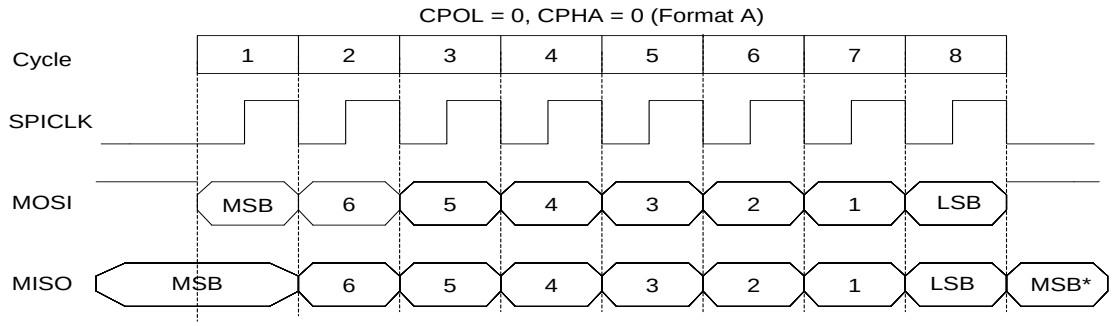


Figure 5-2(a): SPI Transfer Format

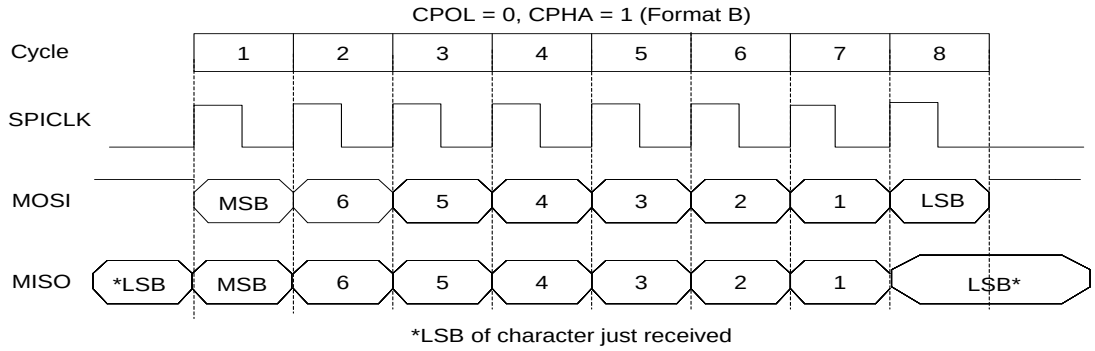


Figure 5-3(b): SPI Transfer Format

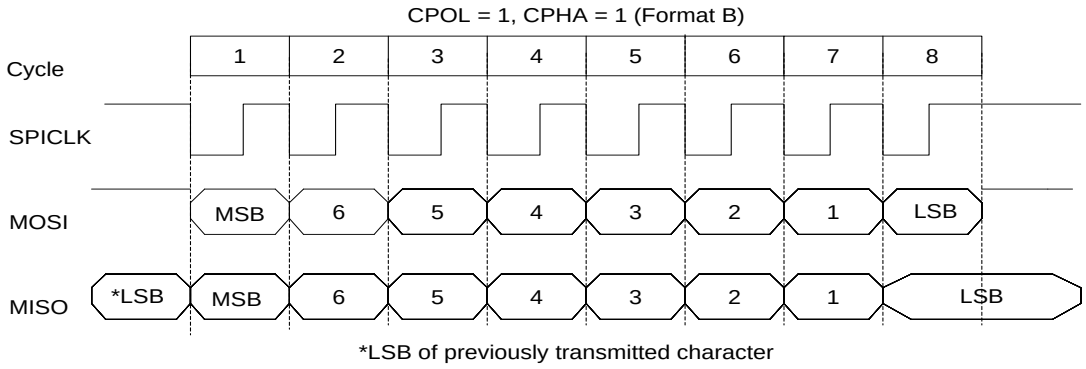


Figure 5-4(c): SPI Transfer Format

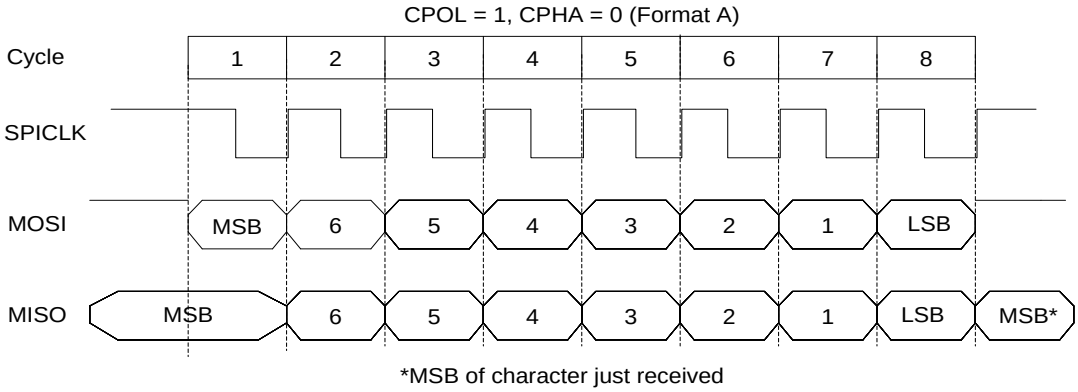


Figure 5-5(d): SPI Transfer Format

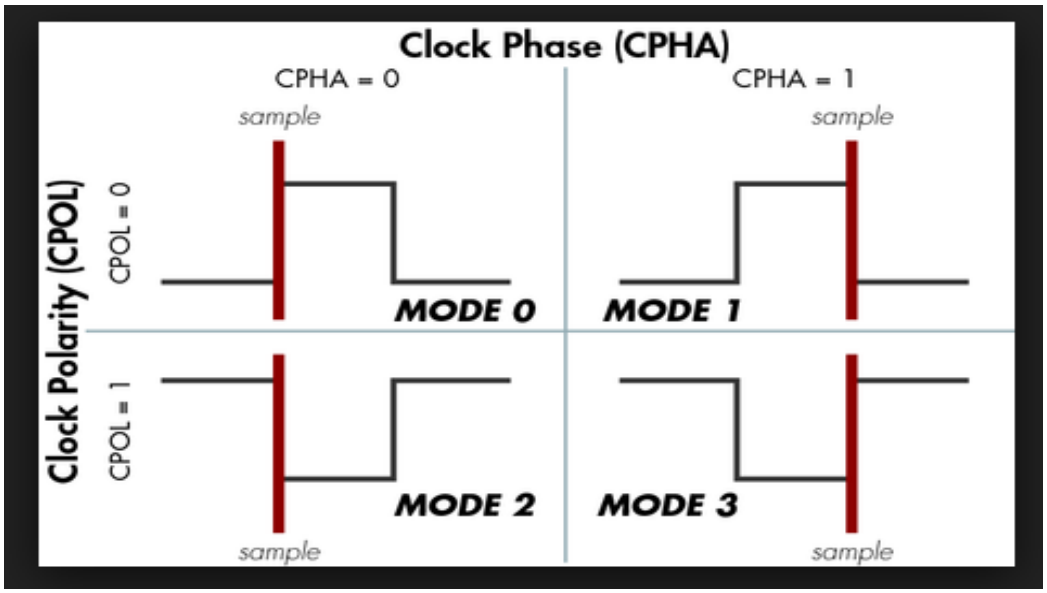


Figure 5-6: SPI Mode

- When length = 0, then hardware (IC) will set the internal length equal to d'96 so fw can read the data of dsp outbuf by 4 times (96*4 = 384 bytes) with crc.
- When crc is disabled, the length setting is ignored, and the state machine is left when spi_cs is from 0 to 1.
- If master crc is not the same as slave crc, then slave will go to error state, master must control spi_cs from 0 to 1 to let slave leave error state to idle state.
- When write to OTP memory, master must wait OTP is ready(0x80), then can continue writing the next byte.

5.1.3 SPI Timing

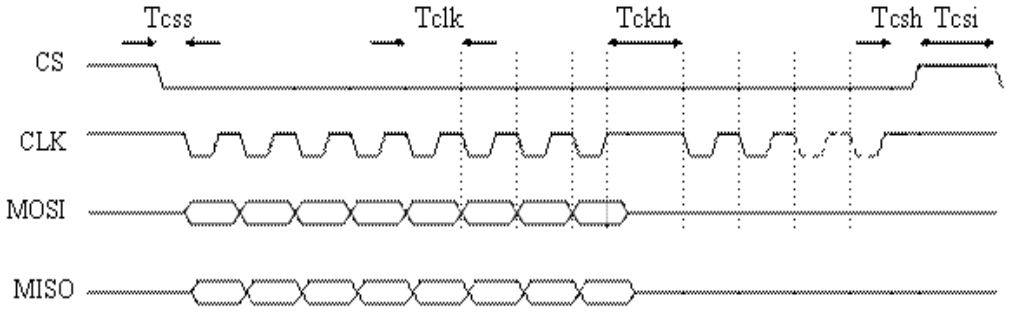


Figure 5-7: SPI Timing

- Tcss >= 3 system clk
- Tcsh >= 3 system clk
- Tcsi >= 3 system clk
- Tckh >= 1.5 spi_clk (about 1.5x4 = 6 system clk) for ram, cfg, buf.
- Tclk >= 4 system clk
- Tckh for OTP

  The first data output of OTP IP needs to be larger than 300ns. So when reading OTP, the Tckh, after finishing to send ADDRL, must be larger than (1.5 spi_clk + 300ns).

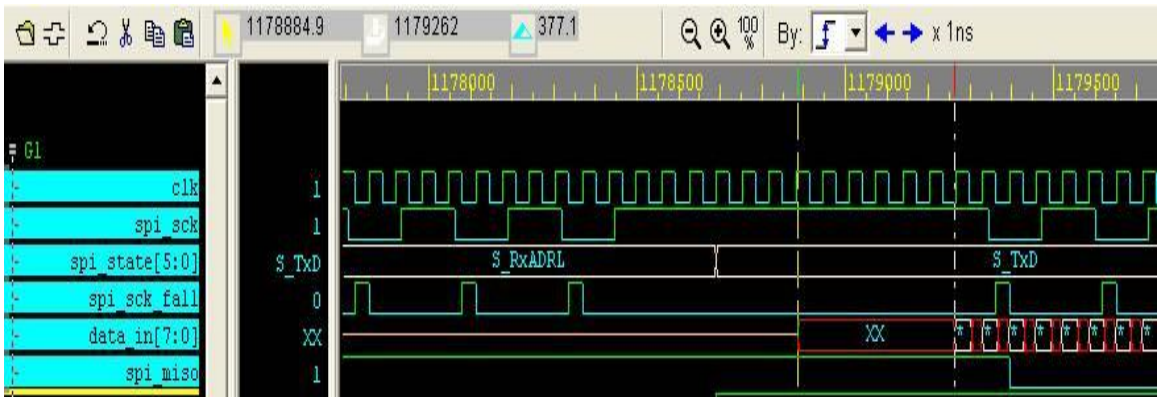


Figure 5-8: Tckh for OTP

5.1.4 SPI with CRC

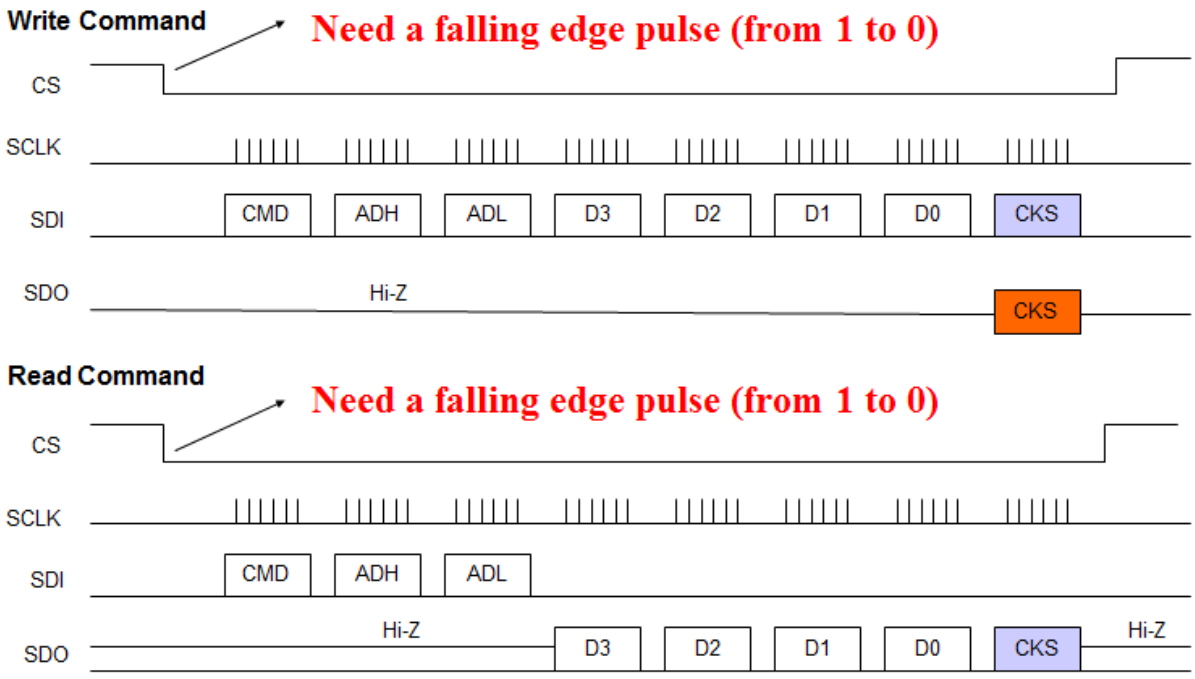


Figure 5-9: SPI with CRC

5.1.5 SPI without CRC

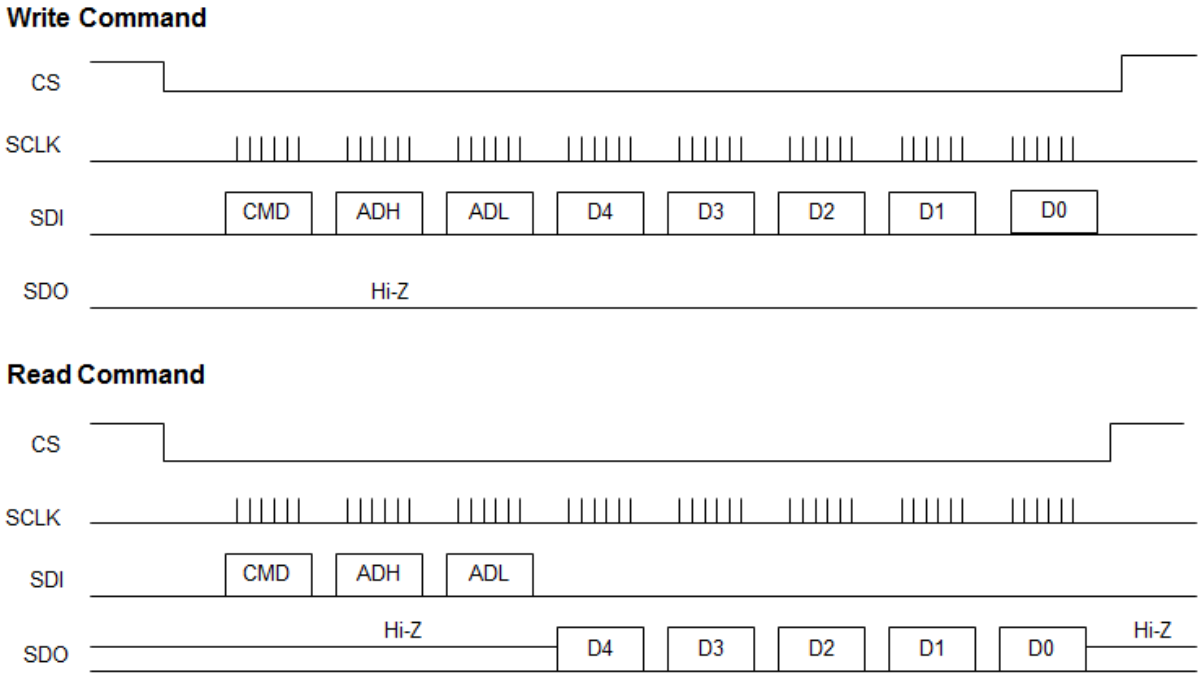


Figure 5-10: SPI without CRC

5.1.6 SPI OTP one byte with CRC

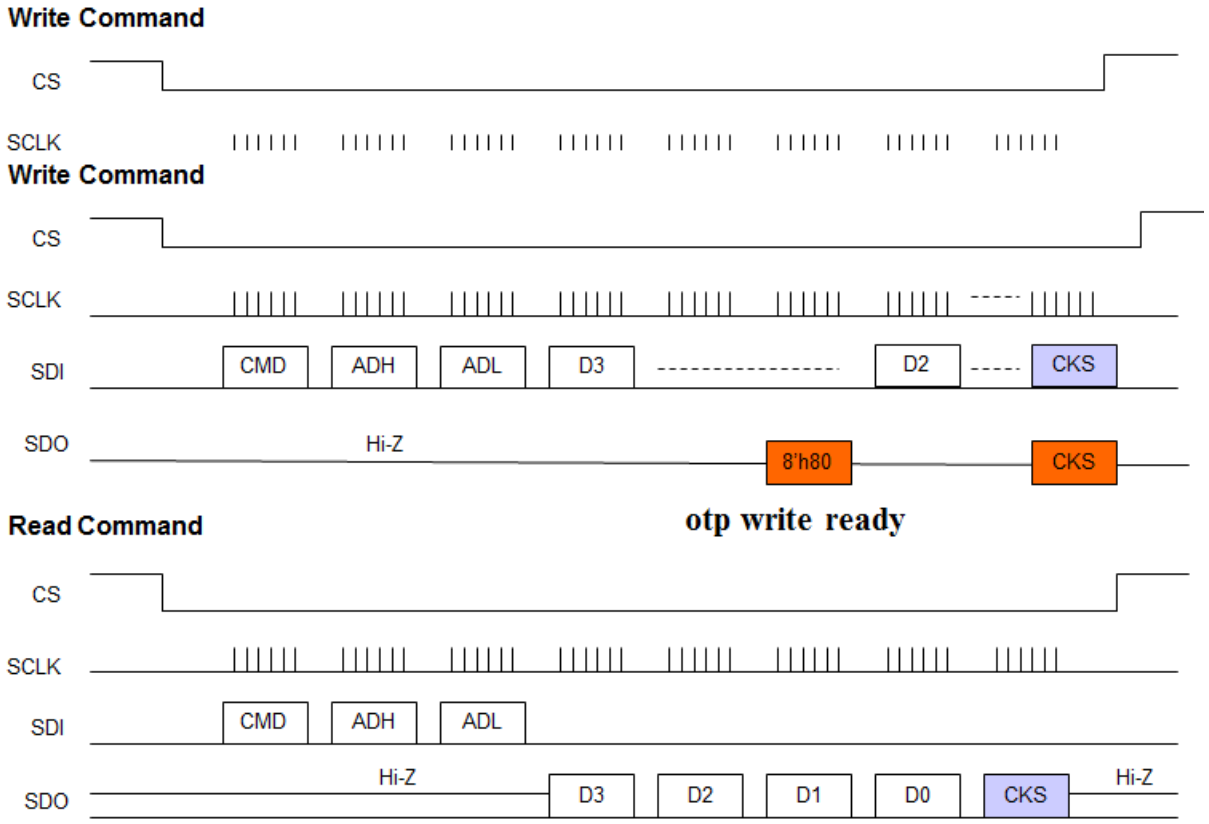


Figure 5-11: SPI OTP one byte with CRC

5.2 I2C Interface

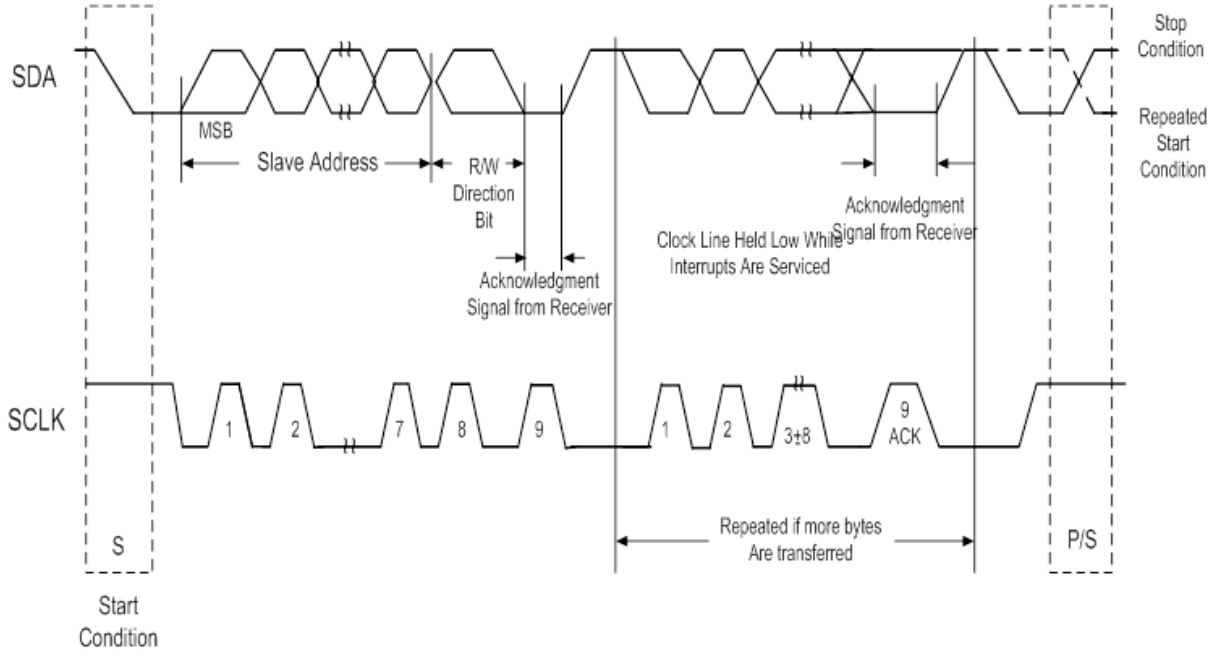


Figure 5-12 aveform of I2C

5.2.1 I2C Write Sequence

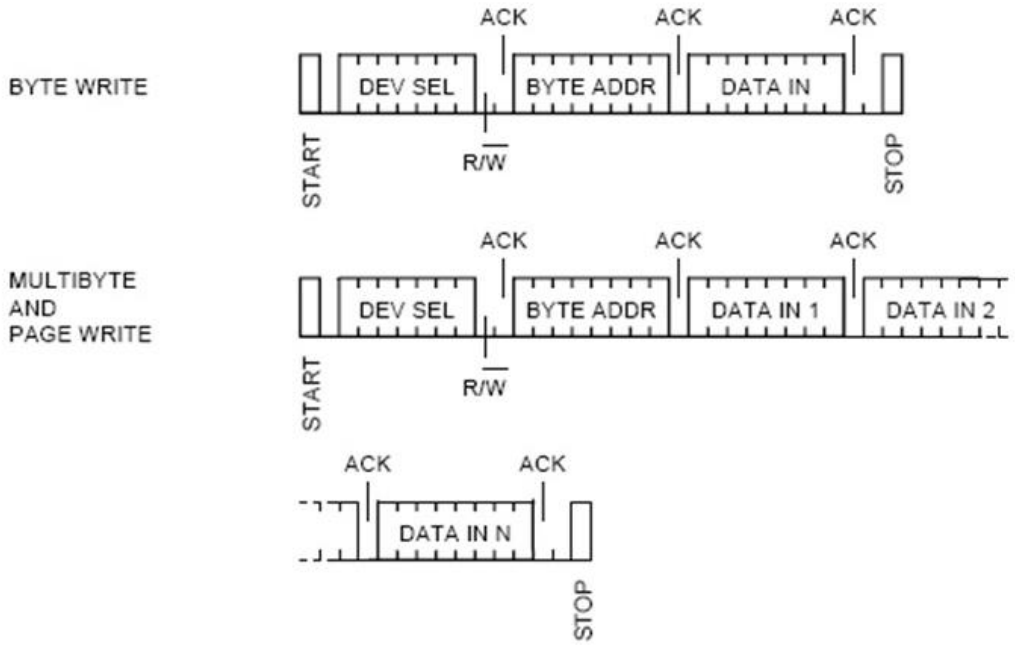


Figure 5-13: I2C Write Sequence (1)

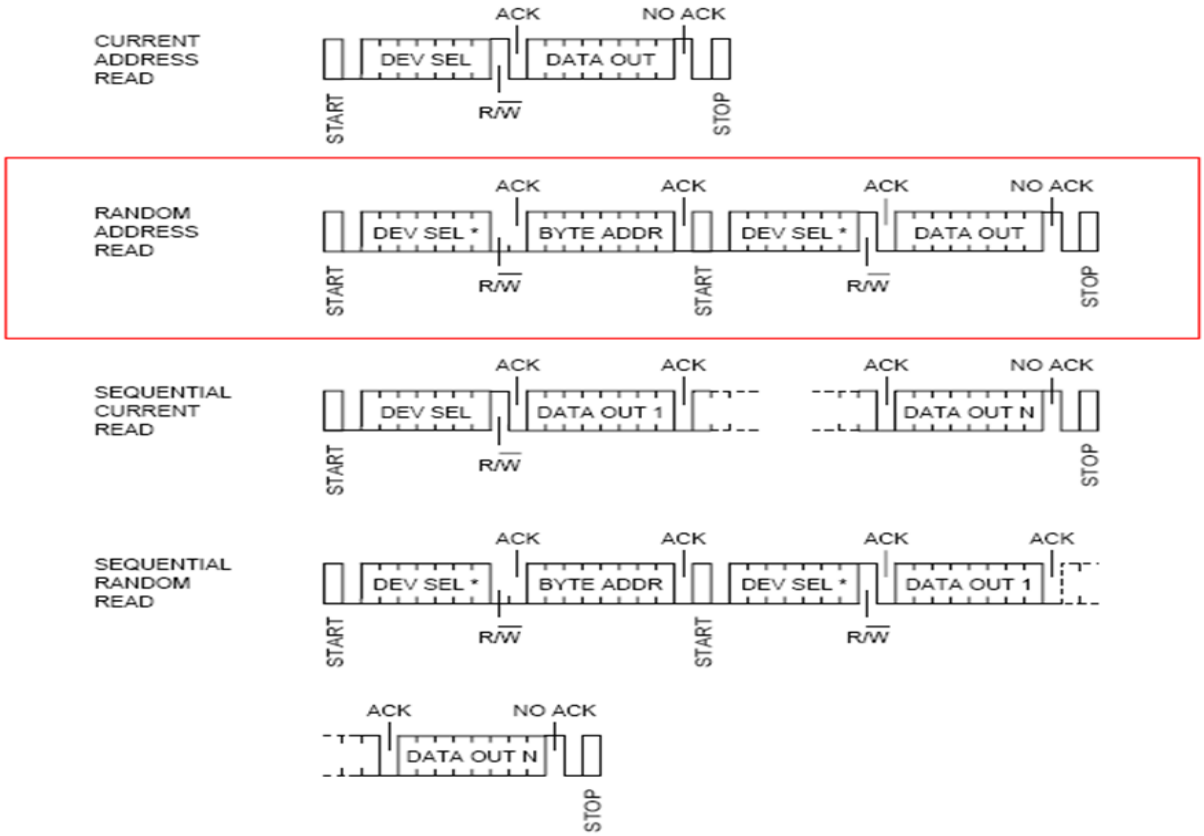


Figure 5-14: I2C Write Sequence (2)

5.2.2 I2C Command

➢ Slave id: default is 0x7F (2-bit from I/O pin: SID1, SID0)

- Iocfg: 0x380d default value: 0xFF,
  so first time I2C is set to default function, then master can reset iocfg to disable default function.
- iocfg[1]: i2c_ref_cs, i2c default is not to reference spi_cs to start i2c.
  set to 1, reference slave id to enable i2c
  spi_cs = 0 is to start so initial master send spi_cs to 0 and mode to 0 to select i2c mode, wait sometime, change spi_cs to 0 to enable i2c r/w.
- iocfg[0] : i2c_lea_cs, i2c default is not reference spi_cs to leave state.
  set to 1 : use stop to leave state
  spi_cs is from 1'b0 to 1'b1 to leave i2c state machine. if i2c_lea_cs is disable, then i2c only reference stop to leave state.

- In write command:

  byte 1 is slave id + R/W (write is 0, read is 1)

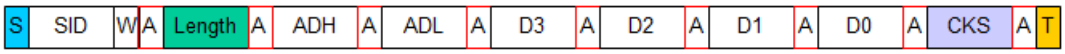
  byte 2 is crc calculation length. When zero, crc is disable;

  when 0xFF, inc_adr_dis is 1 : to disable address increment.

  byte3 is address high : address[15:8]

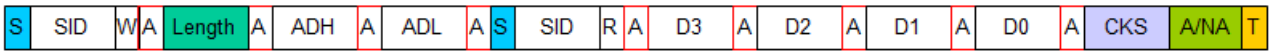
  byte4 is address low : address[7:0]

Write Command

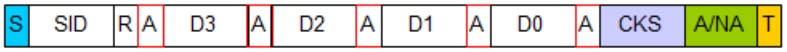


Read Command

Sequential Random address read



Sequential current address read



S : Start ; T : Stop

A : ACK

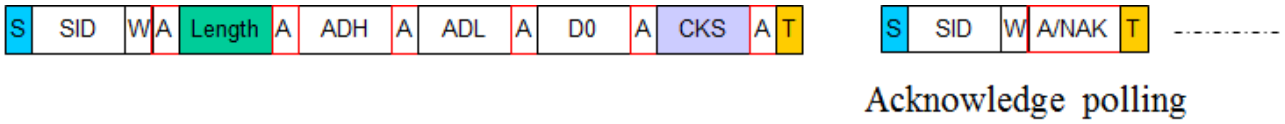
NA : No ACK

Figure 5-15: I2C with CRC

5.2.3 I2C OTP one byte with CRC

Write OTP Command, length = 1 (with crc), 0 (disable crc)

When master write one byte data, and send stop command to start otp write cycle.



If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, the Start bit and control byte must be re-sent. If the cycle is complete, the device will return the ACK and the master can then proceed with the next Read or Write command.

5.3 UART

5.3.1 UART Config

- iocfg : 0x380d default value: 0xFF,
  so first time UART is set to default function, then master can reset iocfg to disable default function.
- iocfg[7]: uart_ref_cs ,uart default is not to reference spi_cs to start uart.
  set to 1, using slave_id to enable uart function
  (spi_cs = 0 is to start. so initial master send spi_cs to 1 and mode to 0 to select uart mode, wait sometime, change spi_cs to 0 to enable uart r/w)
- iocfg[6]: uart_lea_cs, uart default is not to reference spi_cs to leave state.
  set to 1, using timeout to leave state.
  (spi_cs is from 1'b0 to 1'b1 to leave uart state machine. When read, master can use NACK or spi_cs to leave uart state)
- iocfg[5]: uart_bau_en uart defalut is to enable baud rate detection.

5.3.2 UART Slave ID

- slaveid[7:0]: 0x380F
  - slaveid[7]: default is high.
    if this bit is set to high, the general call address (00h) is recognized, otherwise it is ignored.
  - uart_slave_id[7:0] = {slaveid[5:0],slaveio};
  - slave io = {**SID1** pin, **SID0** pin}, 2bit

- iocfg[4:2] : To select time out period
  - 3'd7 : 2^21 * sys_clk (default setting)
  - 3'd6 : 2^20 * sys_clk
  - 3'd5 : 2^19 * sys_clk
  - 3'd4 : 2^18 * sys_clk
  - 3'd3 : 2^17 * sys_clk
  - 3'd2 : 2^16 * sys_clk
  - 3'd1 : 2^15 * sys_clk
  - 3'd0 : 2^14 * sys_clk
  - If default sysclk is 16MHz, then time out is equal to 62.5ns * 2^21 = 131ms.
  - If default sysclk is 4MHz, then time out is equal to 250ns * 2^21 = 524ms.

5.3.3 UART Command

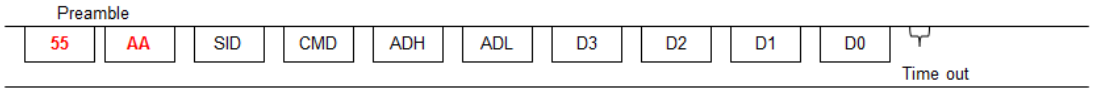
- uart_cmd[7]: inc_adr_dis,
  1: to disable address increment.
  ex: reading dsp_status [DSPRDY, STOP, TRIGCNT] (cfg addr = 16'h387a).
  If DSPRDY is from 0 to 1, then master can read out dsp out buffer data.
- uart_cmd[6:4]: Read/write command
  uart_cmd[6:4] = 3'h1 for read with crc enable
  uart_cmd[6:4] = 3'h2 for write with crc enable
  uart_cmd[6:4] = 3'h3 for read with crc disable
  uart_cmd[6:4] = 3'h4 for write with crc disable
- uart_cmd[3:0]: Read/Write package number
  case1: crc enable, set to 4, master must send out 4byte data + 1byte crc. Then slave will send out 0x5A(ack)/0xA5(nack).
  case2: crc disable, set to 4, master must send out 4byte data. Then slave will not send out 0x5A(ack)/0xA5(nack).
- When length = 0, then hardware (IC) will set the internal length equal to d'96 so FW can read the data of dsp outbuf by 4 times (96*4 = 384 bytes) with crc.
- When crc is disable, the length setting is needed, the state machine is left when time_out.
- uart protocol : start bit + 8bit data + stop bit, no parity bit (10bit)
- 0x55 1byte for baud rate detection
- 0xAA, slave check if baud rate is the same as master.
  - If the same, slave send out 0x5A (Ack), no send out.
  - If not the same, slave send out 0xA5 (NAck), no send out.
- When write command, if slave crc is the same as master crc, then slave send out 0x5A(Ack), not the same, slave send out 0xA5(Nack).
- In write command :
  - If in the time out period, the master sends out another data series, the write state machine will go on writing action. (Address auto increment)
- If time out is got, then the write state machine will go to idle state. Then another write/read command can work.
- otp write time :
  - parameter Tpw_min = 90000 ; //Min Program Pulse Width Time
  - parameter Tpw_max= 110000; //Max Program Pulse Width Time
- In read command:
  - When the read package is end, the master can send out 0x5A for continuing to read

another data package (address auto increment); or 0xA5 for stopping the read action, then the read state machine will go to idle state; or wait time out to idle state.

- If spi_cs is to be referenced, then spi_cs from 0 to 1, then the read state machine will go to idle state.

5.3.4 UART without CRC

Write Command



Read Command

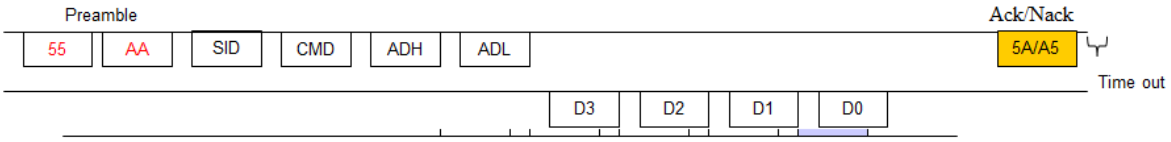
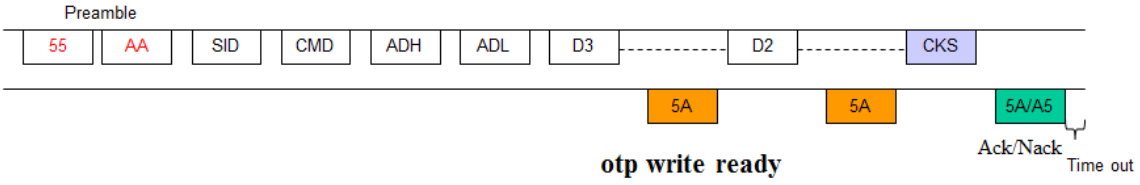


Figure 5-16: UART without CRC

5.3.5 UART OTP one byte with CRC

Write Command



Read Command

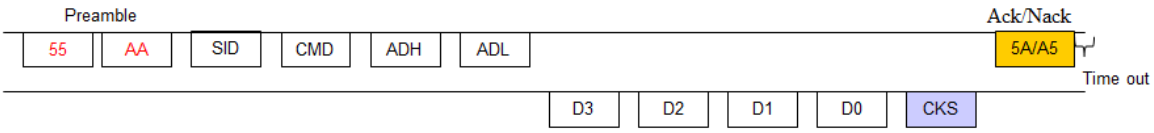


Figure 5-17: UART OTP one byte with CRC

5.4 GPIO

The PL7413 has 9 GPIO pins. These can be configured to be input or output by DSP or register setting.

- locfg[3]: GPIO direction control by DSP or register setting
  1: control by DSP
  0: control by CFG register

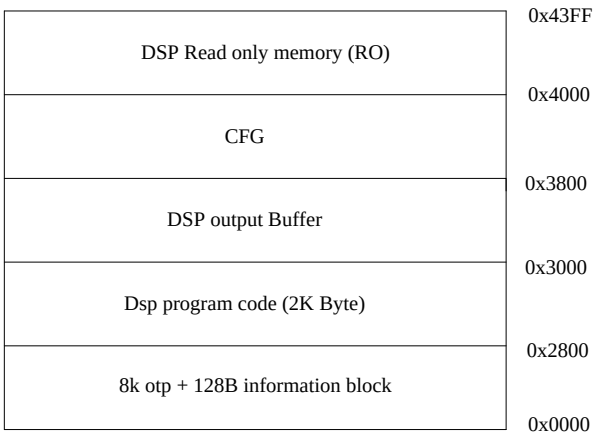
- These can be disabled/enabled:
  reg_pinfunc_P00[1:0]:
  00:GPIO other: special function
- The definitions of reg_pinfunc_P01[1:0] ~ reg_pinfunc_P14[1:0] is the same as reg_pinfunc_P00[1:0].
- The settings can be read out from:
  Address 0x3903: GPIO pins DIR[15:8]
  Address 0x3902: GPIO pins DIR[7:0]
  Address 0x3905: GPIO pins DATA[15:8]
  Address 0x3904: GPIO pins DATA[7:0]
- The GPIO data can be written by DSP firmware, for example:

```
SUBM    R6   xx   GPI_04   R2          // input button GPI_04
STR     GPO_13   R6       0           // Relay output to GPO_13
```

6. Memory Mapping Overview

The PL7413 memory space mapping shown in Figure 6-1 depicts the addressing space and range of each memory macro or register. This memory space is accessible through the SPI/UART/I2C interface of PL7413. The main function of each addressing space is:

- **Configuration (CFG) register**: Various settings, such as DSP options, AVM/MS options and GPIO options, are configured by CFG register. For more details, please see the CFG register section.
- **DSP Buffer**: The calculated energy information located in DSP buffer can be obtained through the SPI/UART/I2C interface of PL7413.
- **DSP Code RAM**: The DSP code RAM stores the program executed by DSP after power on sequence of PL7413 is accomplished.
- **MTP Memory**: MTP (Multi-Time Programmable) memory which is a non-volatile memory stores the DSP code and register configurations. After power-on, the POS (power on sequence) copies the contents of MTP memory to DSP code RAM and CFG registers, respectively. When the POS is done, PL7413 starts to execute based on the DSP code RAM and CFG register settings.



• address decode		real address position
• 0x0000~0x27FF	: 8k OTP + 128B	(0x0000~0x207F)
• 0x2800~0x2FFF	: 2k dsp prog	(0x2800~0x2FFF)
• 0x3000~0x37FF	: 2k dsp buf	(0x3000~0x317f)
• 0x3800~0x3FFF	: 2k cfg	(0x3800~0x39FF)
• 0x4000~0x43FF	: 1k dsp ro	(0x4000~0x43FF)

Figure 6-1: PL7413 Memory Mapping

6.1 MTP memory mapping

The MTP (Multi-Time Programmable) memory which is a non-volatile memory stores the DSP code and register configurations. As shown in Figure 6-2, the MTP memory space is divided into two main sections, which are space for CFG register and for DSP code, respectively.

Due to the one-time programming property of MTP memory, the DSP program section and CFG data section of MTP memory are partitioned into multiple banks for multi-programming times.

The DSP program section of MTP is divided into 3 banks. The size of each bank is 2K Bytes. The CFG data section of MTP is divided into four banks. The size of each bank is 256 bytes.

Only the newest DSP program bank and the newest CFG data bank will be copied into DSP code RAM and CFG registers respectively. It should be programmed from the lowest bank # of DSP/CFG section.

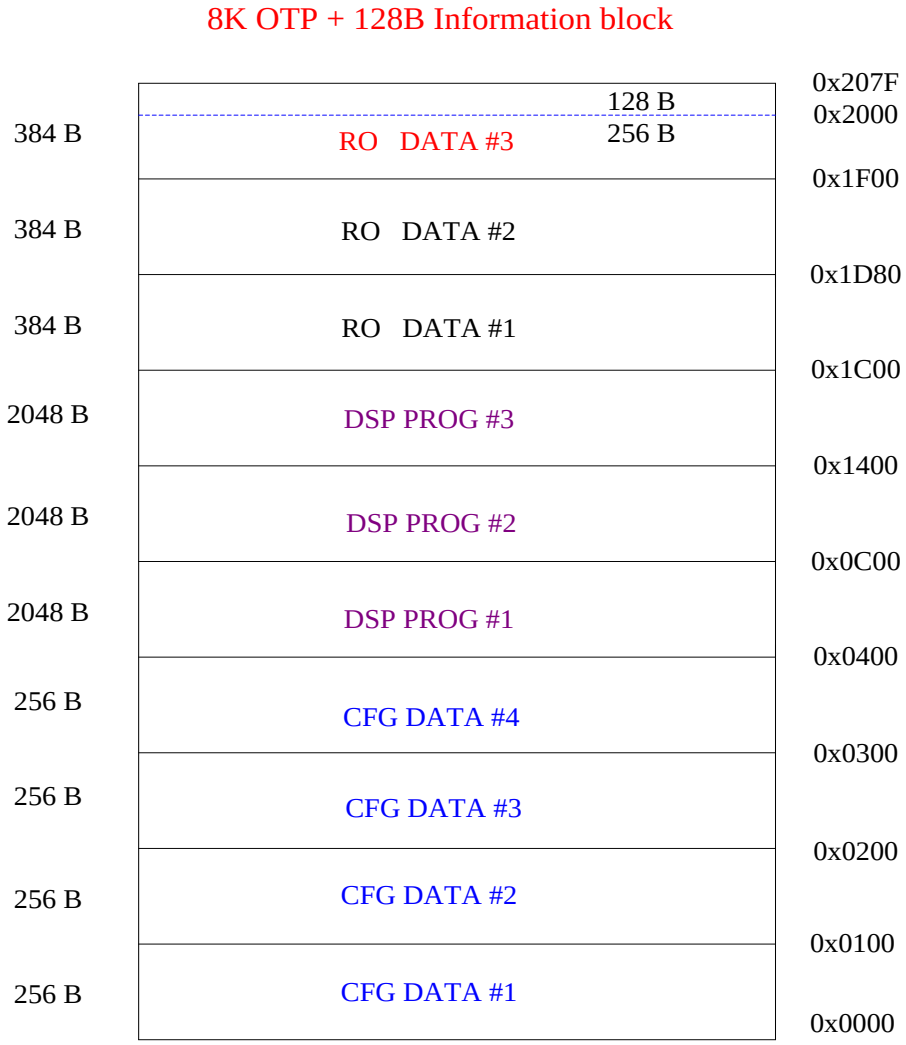


Figure 6-2: MTP Memory Mapping Diagram

7. Power-On Sequence (POS)

When power turns on or external reset is released, the POS copies the MTP memory contents to CFG register and DSP code RAM, respectively. After POS operation, the DSP starts to execute. The POS operating procedure is shown as Figure 7-1.

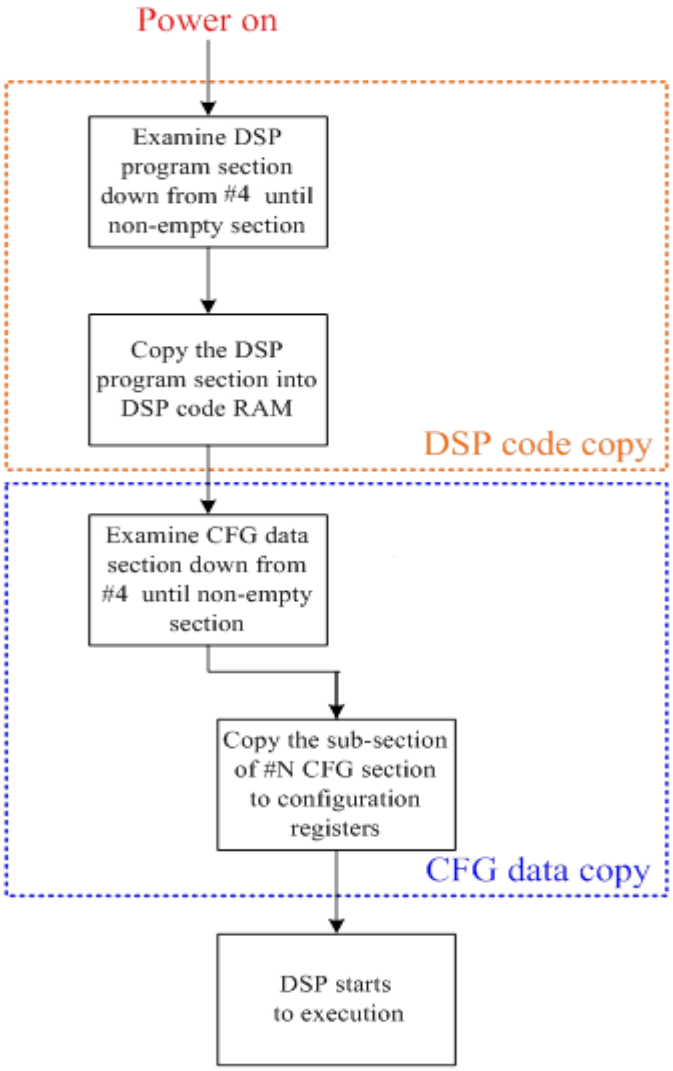


Figure 7-1: POS Sequence

7.1 POS example

Figure 7-2 is a POS example based on the following conditions. In such condition, POS copies CFG DATA #2 from MTP to CFG register, copies DSP bank #3 to DSP code RAM, and copies RO DATA#2 from MTP to RO RAM.

Example Condition:

- CFG DATA 1 and 2 are programmed and bank 3 and 4 are empty.
- DSP PROG 1~3 are programmed.
- RO DATA 1 and 2 are programmed and DATA3 is empty.

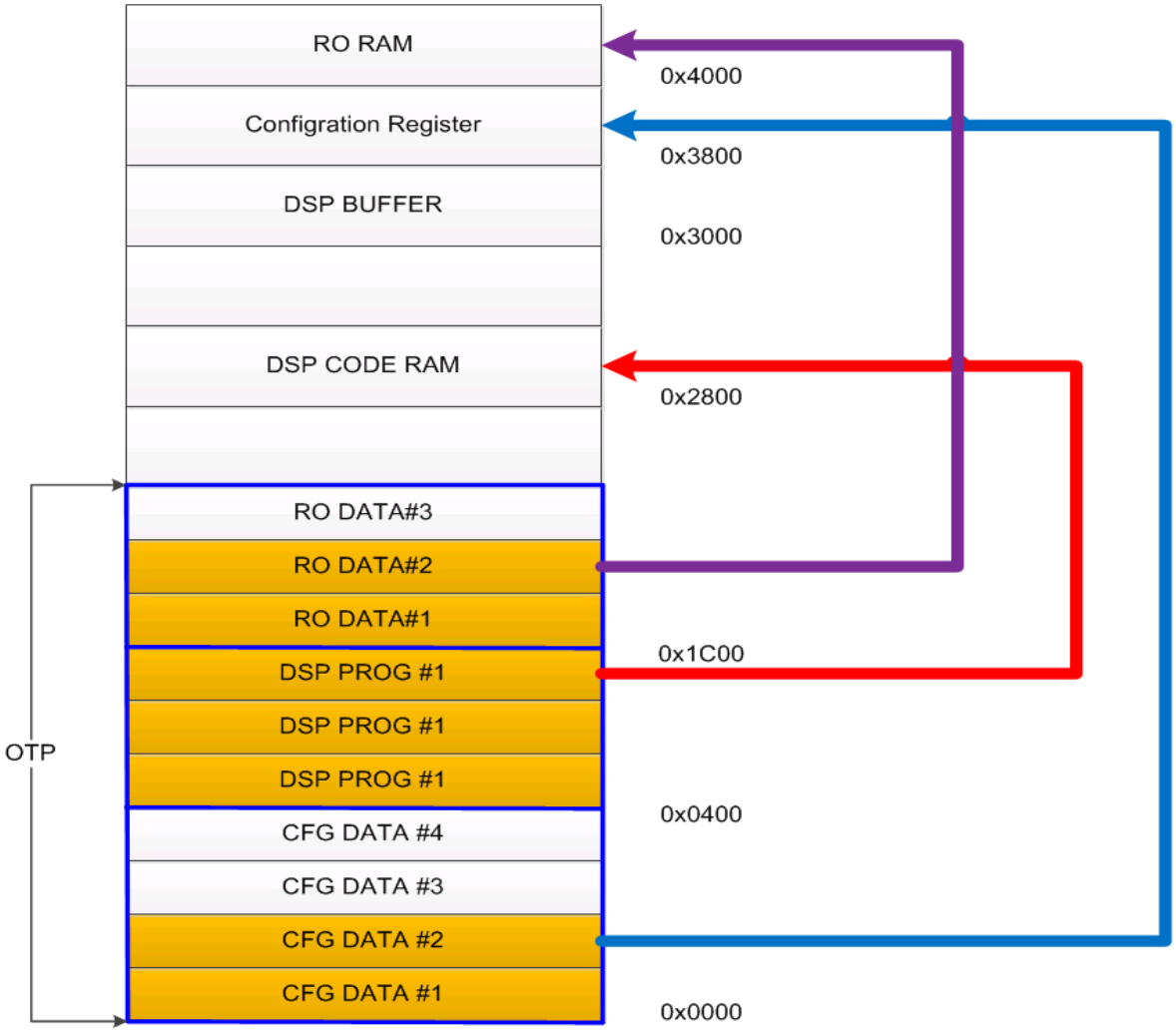


Figure 7-2: POS Sequence Example

8. Configuration (CFG) Registers

The configuration (CFG) registers located at 0x3800 are classified into system registers, analog registers and AFE parameter registers:

- System registers: These registers are used to configure miscellaneous function of whole system.
- AFE parameter registers: These registers are used to configure AFE control module.
- Analog registers: These registers are used to configure analog module, ex: power down, oscillator, and ADC, etc.

Since the contents of the CFG registers are copied from MTP memory after power up or external reset, their initial values depend on the contents of MTP memory. Consequently, the initial value of CFG registers will not be mentioned.

Table 8-1：System Registers

System Registers				
Addr	**Mnemonic**	**Bits**	**Description**	
0x3800	**SYSCFG**	**7:0**	**Default:0x00**	**Access:RW**
	SW_RST	7:6	2’b10: Issue software reset. 2’b11: Enable DSP IR parity error reset signal	
	pclk_div2	5:4	2’b10: enable per clk to divider by 2	
		3:2	2’b10: enable test mode and apc_mrcb	
	testmode	1	SYSCFG[3:2] = 2’b10,0: enable 1: disable	
	apc_mrcb	0	SYSCFG[3:2] = 2’b10,0:enable 1:disable	
0x3801	**ADCCFG**	**7:0**	**Default:0x00**	**Access:RW**
	ADCEN	7	0: ADC Clock disable 1: ADC Clock enable	
	ADC_SEL	6	0: ADC RAW BIT SEL(from IO pad) 1:ADC RAW BIT SEL(from analog part)	
		5:4	Reserved	
	ADCDIV	3:0	ADC clock division ADC clock = system_clock/(ADCDIV+1)	
0x3802	**DSPCFG**	**7:0**	**Default:0x00**	**Access:RW**
	DSP_EN	7	0: DSP Disable 1: DSP Enable	
	AUTO_CLR	6	0: DSPRDY auto clr is enable(spi_cs is from 0 to 1) 1: DSPRDY auto clr is disable	
	CLR_Flag	5	0: no clr action 1:set to 1 to clr DSPRDY, hardware will auto clr this bit	
	DSP_TM	4	0: DSP Normal mode	

System Registers				
Addr	**Mnemonic**	**Bits**	**Description**	
			1: DSP Test mode	
	DSPDIV	3:0	DSP clock division DSP clock = system_clock/(DSPDIV+1)	
0x3803	**CFGReg_B0**	**7:0**	**Default:0x00**	**Access:RW**
			DSP configuration register, bit0~bit7	
0x3804	**CFGReg_B1**	**7:0**	**Default:0x00**	**Access:RW**
			DSP configuration register, bit8~bit15	
0x3805	**LENG**	**7:0**	**Default:0x60**	**Access:RW**
			For setting spi/uart slave read/write byte length	
0x3806	**WDTCFG**	**7:0**	**Default:0xFF**	**Access:RW**
	WDT_SEL	7:5	(0:2^13 , 1 : 2^14 , 2 : 2^15, 3:2^16 , 4:2^17 , 5 :2^18 , 6:2^19 , 7:2^20)	
		4	Reserved	
	WDT_RST	3	active high or active low (1 for active high)	
		2:1	Reserved	
	WDT_CLR	0	1 for wdt counter reset	
0x3807	**OTP_BIST_DATA**	**7:0**	**Default:0x00**	**Access:RW**
			If otp all data are the same. Write the same data value into CFG 0x3807	
0x3808	**FlagSel_CTL**	**7:0**	**Default:0x0F**	**Access:RW**
	OTP_BIST_TEST	7	1 for OTP BIST TEST MODE, length = 0~4 0 for normal mode, length=0~0x207f	
	OTP_BIST_EN	6:5	2'b10 , then otp_bist is enable	
		4:2	Reserved	
	DSP_FLAG_SEL	1:0		
0x3809	**SampleCnt_B0**	**7:0**	**Default:0x00**	**Access:RW**
			Sample count setting, Byte-0	
0x380A	**SampleCnt_B1**	**7:0**	**Default:0x00**	**Access:RW**
			Sample count setting, Byte-1	
0x380B	**delaycnt_B0**	**7:0**	**Default:0x40**	**Access:RW**
			OTP delay count setting, Byte-0	
0x380C	**delaycnt_B1**	**7:0**	**Default:0x06**	**Access:RW**
			OTP delay count setting, Byte-1 **system clk divides delaycnt must be larger than 300ns**	
0x380D	**iocfg**	**7:0**	**Default:0xFF**	**Access:RW**
	uart_ref_cs	7	Uart reference spi_cs to start 0: reference spi_cs	
	uart_lea_cs	6	Uart reference spi_cs to leave 0: reference spi_cs	

System Registers				
Addr	**Mnemonic**	**Bits**	**Description**	
	uart_bau_en	5	1: enable baud rate detection 0: disable	
		4	Reserved	
	GPIO_DIR_SEL	3	GPIO direction control 0: CFG 1: DSP	
	gen_call_read_en	2	1 : for gen_cal , disable read function(default) 0 : for gen_cal , enable read function	
	i2c_ref_cs	1	I2C reference spi_cs to start 0: reference spi_cs	
	i2c_lea_cs	0	I2C reference spi_cs to leave 0: reference spi_cs	
0x380E	**clkcfg**	**7:0**	**Default:0x73**	**Access:RW**
		7	Reserved	
	uart_to_cfg	6:4	uart time out period 3'b111:2^21*system clk(16Mhz = 125ms) 3'b110:2^20*system clk 3'b101:2^19*system clk 3'b100:2^18*system clk 3'b011:2^17*system clk 3'b010:2^16*system clk 3'b001:2^15*system clk 3'b000:2^14*system clk	
	div_sel	3:2	anti-clock fail detection circuit clear fail detection count(frequency select)	
	dlysel	1:0	anti-clock fail detection circuit fail detection and switch period	
0x380F	**SLAVEID**	**7:0**	**Default:0x7F**	**Access:RW**
	gen_call_en	7	cen_call enable 1:enable	
		6	Reserved	
	salve_id	5:0	I2C slave id = {slaveid[4:0],slaveio} Uart slave id = {slaveid[5:0],slaveio}	
0x3810	**I2F_IDATA_R_B0**	**7:0**	**Default:0x00**	**Access:RW**
			I2F DATA by CFG	
0x3811	**I2F_IDATA_R_B1**	**7:0**	**Default:0x00**	**Access:RW**
			I2F DATA by CFG	
0x3812	**I2F_IDATA_R_B2**	**7:0**	**Default:0x00**	**Access:RW**
			I2F DATA by CFG	
0x3813	**I2F_IDATA_R_B3**	**7:0**	**Default:0x00**	**Access:RW**

System Registers				
Addr	**Mnemonic**	**Bits**	**Description**	
			I2F DATA by CFG	
0x3814	**I2F_IDATA_R_B4**	**7:0**	**Default:0x00**	**Access:RW**
			I2F DATA by CFG	
0x3815	**I2F_IDATA_R_B5**	**7:0**	**Default:0x00**	**Access:RW**
			I2F DATA by CFG	
0x3816	**I2F_CTL**	**7:0**	**Default:0x00**	**Access:RW**
		7	I2F RADIX and SIGN SELECTION 0: set by register, 1: set by dsp wo	
		6	I2F DATA SELECTION 0: set by register, 1: set by dsp wo	
		5	I2F SIGN Value	
		4:0	I2F RADIX Value	
0x381A	**CORDIC_SIN_B0**	**7:0**	**Default:0x00**	**Access:RW**
			CORDIC SIN Low byte	
0x381B	**CORDIC_SIN_B0**	**7:0**	**Default:0x00**	**Access:RW**
			CORDIC SIN High byte	
0x381C	**CORDIC_COS_B0**	**7:0**	**Default:0x00**	**Access:RW**
			CORDIC COS Low byte	
0x381D	**CORDIC_COS_B0**	**7:0**	**Default:0x00**	**Access:RW**
			CORDIC COS High byte	
0x381E	**GPIO_DIR_B0**	**7:0**	**Default:0x00**	**Access:RW**
			GPIO direction control,0: input 1: output	
0x381F	**GPIO_DIR_B1**	**7:0**	**Default:0x00**	**Access:RW**
			GPIO direction control,0: input 1: output	
0x3824	**I Channel Gain**	**7:0**	**Default:0x00**	**Access:RW**
		7	Reserved	
	Gain1	6:4	I1 gain	
		3	Reserved	
	Gain0	2:0	I0 gain	
0x3825	**I Channel Gain**	**7:0**	**Default:0x00**	**Access:RW**
		7	Reserved	
	Gain3	6:4	I3 gain	
		3	Reserved	
	Gain2	2:0	I2 gain	
0x3826	**V Channel Gain**	**7:0**	**Default:0x00**	**Access:RW**
		7	Reserved	
	Gain5	6:4	V1 gain	
		3	Reserved	
	Gain4	2:0	V0 gain	
0x3827	**V Channel Gain**	**7:0**	**Default:0x00**	**Access:RW**

System Registers				
Addr	**Mnemonic**	**Bits**	**Description**	
		7	Reserved	
	Gain7	6:4	V3 gain	
		3	Reserved	
	Gain6	2:0	V2 gain	
0x3834	**MAST_CTL_B0**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	SPI/I2C mode: eeprom byte length(low byte) Uart mode:bit[6:0] is uart send out package length	
0x3835	**MAST_CTL_B1**	**7:0**	**Default:0x00**	**Access:RW**
	mast_haddr_en	7	Slave device need 2 byte address 1:enable(2 byte) 0:disable(1 byte)	
		6:0	SPI/I2C mode: eeprom byte length(high byte)	
0x3836	**MAST_CTL_B2**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	Reserved	
0x3837	**MAST_SID**	**7:0**	**Default:0xD0**	**Access:RW**
		7:1	I2C mode: bit[7:1] for setting exteranl slave i2c eeprom device id Uart mode: bit[7:4] for cpol cpha control bit[7] = cpol bit[6] = cpha bit[5:4] 2'b11	
		0	Reserved	
0x3838	**MAST_HADR**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	SPI/I2C mode: for setting external eeprom haddr Uart mode: for setting uart master read dsp outbuf haddr	
0x3839	**MAST_LADR**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	SPI/I2C mode: for setting external eeprom laddr Uart mode: for setting uart master read dsp outbuf laddr	
0x383A	**spim_cmd0**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	SPI/I2C mode: spi master WREN command(8'h06) Uart mode: BitWidthNum_master low byte	
0x383B	**spim_cmd1**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	SPI/I2C mode: spi master WRITE command(8'h02) Uart mode:bits[5:0] is BitWidthNum_master high byte	
0x383C	**spim_cmd2**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	SPI/I2C mode: spi master READ command(8'h03) Uart mode:bit[7] uart master enable Bit[4:0] BitWidthDen_master	
0x3890	**IR_CFG_B0**	**7:0**	**Default:0x00**	**Access:RW**
	ir_filter_length	7:0		
0x3891	**IR_CFG_B1**	**7:0**	**Default:0x00**	**Access:RW**
	ir_bit_num	7:2	bit[5:0]	
	ir_filter_length	1:0		

System Registers				
Addr	**Mnemonic**	**Bits**	**Description**	
0x3892	**IR_CFG_B2**	**7:0**	**Default:0x00**	**Access:RW**
	MSB_SEL	7	1: MSB first 0: LSB first	
	ir_invert	6	1: invert	
	ir_enable	5:4	00: disable 01: msp3_ir enable 10: bi_phase_ir enable 11: pcm_ir enable	
	ir_start_bit	3	1: ir type have start bit 0: ir type no start bit	
	ir_valid	2		
	ir_in_mux	1	1: UART_RX 0: ir_mod_in	
	ir_bit_num	0	bit[6]	
0x3893	**IR_T_BASE_B0**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	ir time base high byte	
0x3894	**IR_T_BASE_B1**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	ir time base high byte	
0x3895	**IR_T_TH**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	For Start_bit, TH = IR_T_TH[7:0] *(2)^ IR_T_GAIN[5:3] For logic bit, TH = IR_T_TH[7:0] *(2)^(IR_T_GAIN[2:0])	
0x3896	**IR_LEAD_CFG**	**7:0**	**Default:0x00**	**Access:RW**
		7:0		
0x3897	**IR_LOGIC_CFG_B0**	**7:0**	**Default:0x00**	**Access:RW**
		7:0		
0x3898	**IR_LOGIC_CFG_B1**	**7:0**	**Default:0x00**	**Access:RW**
		7:0		
0x3899	**IR_SPACE_CFG**	**7:0**	**Default:0x00**	**Access:RW**
		7:0		
0x389A	**IR_T_GAIN**	**7:0**	**Default:0x00**	**Access:RW**
		7:0		
0x389C	**IOMUX0**	**7:0**	**Default:0x00**	**Access:RW**
	reg_pinfunc_P03	7:6	Normal mode: 00:GPIO 10:wdt_rst 11:mode_latch Analog mode: 00:DG_BGD_3V 01:DG_PG_3V 10:bit_i1	

System Registers				
Addr	**Mnemonic**	**Bits**	**Description**	
			11:DG_OSC_LOW_GD	
	reg_pinfunc_P02	5:4	00:GPIO 11:BD option0	
	reg_pinfunc_P01	3:2	00:GPIO Others:SPI_DX/TXD/SDA	
	reg_pinfunc_P00	1:0	00:GPIO 01:IR_in 11:CS	
0x389D	**IOMUX1**	**7:0**	**Default:0x00**	**Access:RW**
	reg_pinfunc_P07	7:6	00:GPIO 10:SPI_SSN 11:II_in	
	reg_pinfunc_P06	5:4	00:GPIO 10:IR_in 11:VI_in	
	reg_pinfunc_P05	3:2	00:GPIO 11:IR_in	
	reg_pinfunc_P04	1:0	00:GPIO 01: IR_in 10:wdt_rst 11:SPI_SCLK/I2C_SID	
0x389E	**IOMUX2**	**7:0**	**Default:0x00**	**Access:RW**
	reg_pinfunc_P11	7:6	00:GPIO Others:SPI_DI/UART_RXD/I2C_SID0	
	reg_pinfunc_P10	5:4	00:GPIO Others:SPI_SCLK/I2C_SCL	
	reg_pinfunc_P09	3:2	00:GPIO 01:ir_data_decod 10:SPI_SSN 11:SPI_DI	
	reg_pinfunc_P08	1:0	Normal mode: 00:GPIO 01:ir_data_valid 10:wdt_rst 11:ADC_CLK_IN Analog mode: 00:DG_CLK_16M_3V 01:DG_CK_OSC2_3V 10:DG_CLKOSC_3V 11:ADC_CLK	

System Registers				
Addr	**Mnemonic**	**Bits**	**Description**	
0x389F	**IOMUX3**	**7:0**	**Default:0x00**	**Access:RW**
	reg_pinfunc_P15	7:6	Reserved	
	reg_pinfunc_P14	5:4	00:GPIO 11:BD option2	
	reg_pinfunc_P13	3:2	00:GPIO 11:s_st_error	
	reg_pinfunc_P12	1:0	Normal mode: 00:GPIO 01:ir_ready 10:wdt_rst 11:s_st_error Analog mode: 00:DG_AVDD3_VD_3V 01:DG_VIND_PG 10:bit_v1 11:DG_OSC_LOW_GD	
0x3902	**GPIO_DIR**	**7:0**	**Default:**	**Access:R**
		7:0	GPIO_DIR low byte	
0x3903	**GPIO_DIR**	**7:0**	**Default:**	**Access:R**
		7:0	GPIO_DIR high byte	
0x3904	**GPIO_DATA**	**7:0**	**Default:**	**Access:R**
		7:0	GPIO_DATA low byte	
0x3905	**GPIO_DATA**	**7:0**	**Default:**	**Access:R**
		7:0	GPIO_DATA high byte	
0x3906	**AGC1**	**7:0**	**Default:**	**Access:R**
		7:0		
0x3907	**AGC2**	**7:0**	**Default:**	**Access:R**
		7:0		
0x3908	**LOOPCNT_L**	**7:0**	**Default:**	**Access:R**
		7:0		
0x3909	**LOOPCNT_H**	**7:0**	**Default:**	**Access:R**
		7:0		
0x390A		**7:0**	**Default:**	**Access:R**
	Status	7:0		
0x390B		**7:0**	**Default:**	**Access:R**
	c_crc_get	7:0		
0x390C		**7:0**	**Default:**	**Access:R**
	c_crc_cal	7:0		
0x390D		**7**	**Default:**	**Access:R**
	s_crc_kp	7		

System Registers				
Addr	**Mnemonic**	**Bits**	**Description**	
0x390E		**7**	**Default:**	**Access:R**
	ready_keep	7		
0x390F		**7**	**Default:**	**Access:R**
	clkmod	7		
0x3910	**FlagDSP_B0**	**7:0**	**Default:**	**Access:R**
		7:2	FlagDSP[7:2]	
0x3911	**FlagDSP_B1**	**7:0**	**Default:**	**Access:R**
		7:0	FlagDSP[15:8]	
0x3912	**FlagDSP_B2**	**7:0**	**Default:**	**Access:R**
		7:0	FlagDSP[23:16]	
0x3913	**FlagDSP_B3**	**7:0**	**Default:**	**Access:R**
		7:0	FlagDSP[31:24]	
0x3914	**FlagReg_B0**	**7:0**	**Default:**	**Access:R**
		7:0	FlagReg [7:0]	
0x3915	**FlagReg_B1**	**7:0**	**Default:**	**Access:R**
		7:0	FlagReg [15:8]	
0x3916	**FlagReg_B2**	**7:0**	**Default:**	**Access:R**
		7:0	FlagReg [23:16]	
0x3917	**FlagReg_B3**	**7:0**	**Default:**	**Access:R**
		7:0	FlagReg[31:24]	
0x3918	**BitWidthNum_B0**	**7:0**	**Default:**	**Access:R**
		7:0	BitWidthNum[7:0]	
0x3919	**BitWidthNum_B1**	**5:0**	**Default:**	**Access:R**
		5:0	BitWidthNum[13:8]	
0x391A	**BitWidthDen**	**4:0**	**Default:**	**Access:R**
		4:0	BitWidthDen[4:0]	
0x391C	**I2F_FDATA_B0**	**7:0**	**Default:**	**Access:R**
		7:0		
0x391D	**I2F_FDATA_B1**	**7:0**	**Default:**	**Access:R**
		7:0		
0x391E	**I2F_FDATA_B2**	**7:0**	**Default:**	**Access:R**
		7:0		
0x391F	**I2F_FDATA_B3**	**7:0**	**Default:**	**Access:R**
		7:0		
0x3926		**7**	**Default:**	**Access:R**
	AFETRIG	7		
0x3927	**AFEV1_B0**	**7:0**	**Default:**	**Access:R**
		7:0	AFEV1[7:0]	
0x3928	**AFEV1_B1**	**7:0**	**Default:**	**Access:R**

System Registers				
Addr	**Mnemonic**	**Bits**	**Description**	
		7:0	AFEV1[15:8]	
0x3929	**AFEV1_B2**	**7:0**	**Default:**	**Access:R**
		7:0	AFEV1[23:16]	
0x392A	**AFEI1_B0**	**7:0**	**Default:**	**Access:R**
		7:0	AFEI1[7:0]	
0x392B	**AFEI1_B1**	**7:0**	**Default:**	**Access:R**
		7:0	AFEI1[15:8]	
0x392C	**AFEI1_B2**	**7:0**	**Default:**	**Access:R**
		7:0	AFEI1[23:6]	
0x393D	**bist_result**	**1:0**	**Default:**	**Access:R**
		1:0	bist_result	
0x393E	**bist_crc_out_B0**	**7:0**	**Default:**	**Access:R**
		7:0	bist_crc_out[7:0]	
0x393F	**bist_crc_out_B1**	**7:0**	**Default:**	**Access:R**
		7:0	bist_crc_out[15:8]	

Table 8-2：AFE Related Registers

AFE related Registers				
Addr	**Mnemonic**	**Bits**	**Description**	
0x3840	**AFECFG0_B0**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	Reserved	
0x3841	**AFECFG0_B1**	**7:0**	**Default:0x00**	**Access:RW**
	EN_COMP	7	=1: sinc3 compensation filter enable	
	COMP_COEF	6:0	sinc3 compensation filter coefficient Q2.5 (default=0x30=1.5)	
0x3842	**AFECFG0_B2**	**7:0**	**Default:0x00**	**Access:RW**
		7:5	Reserved	
	INTP test mode	4	=1 : V0/I0 interpolation test mode	
	ADC_CLK_PHSI	3	I channel adc_bit posedge(=1)/negedge(=0) selection	
	ADC_CLK_PHSV	2	V channel adc_bit posedge(=1)/negedge(=0) selection	
	EN_FIR_SEL	1:0	sinc3 compensation FIR tap select (=0 : disable; =1 : 1-tap; =2 : 2-tap; =3 : 2-tap)	
0x3843	**AFECFG0_B3**	**7:0**	**Default:0x00**	**Access:RW**
		7	Reserved	
	DCF_sel	6:5	OSR selection (=0 : OSR64; =1 : OSR128; =2 : OSR256; =3 : OSR512)	
	HPF_sel	4	high-pass filter scale selection (=0: 1/512; =1: 1/256)	
		3:2	Reserved	
	INT_sel_I	1:0	integrator I channel scale selection (=0: 1/16; =1: 1/32; =2: 1/64; =3: 1/128)	
0x3844	**AFECFG1_B0**	**7:0**	**Default:0x00**	**Access:RW**
		7	Reserved	
	MCH	6:5	mux channel number 4MUX 8MUX 00: 1CH 1CH 01: 2CH 2CH 10: 3CH 4CH 11: 4CH 8CH	
		4:0	Reserved	
0x3845	**AFECFG1_B1**	**7:0**	**Default:0x00**	**Access:RW**
	ISID2	7:6	I channel Slot ID2(bit[1:0])	
	ISID1	5:3	I channel Slot ID1	
	ISID0	2:0	I channel Slot ID0	
0x3846	**AFECFG1_B2**	**7:0**	**Default:0x00**	**Access:RW**
		7:4	Reserved	
	ISID3	3:1	I channel Slot ID3	
	ISID2	0	I channel Slot ID2(bit[2])	
0x3847	**AFECFG1_B2**	**7:0**	**Default:0x00**	**Access:RW**

AFE related Registers				
Addr	**Mnemonic**	**Bits**	**Description**	
		7:0	Reserved	
0x3848	**AFECFG2_B0**	**7:0**	**Default:0x00**	**Access:RW**
		7:2	Reserved	
	ICHEN	1	=1: I Decimator Enable	
	VCHEN	0	=1: V Decimator Enable	
0x3849	**AFECFG2_B1**	**7:0**	**Default:0x00**	**Access:RW**
	VSID2	7:6	V channel slot ID2(bit[1:0])	
	VSID1	5:3	V channel slot ID1	
	VSID0	2:0	V channel slot ID0	
0x384A	**AFECFG2_B2**	**7:0**	**Default:0x00**	**Access:RW**
		7:4	Reserved	
	VSID3	3:1	V channel slot ID3	
	VSID2	0	V channel slot ID2(bit[2])	
0x384B	**AFECFG2_B2**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	Reserved	
0x384C	**AFECFG3_B0**	**7:0**	**Default:0x00**	**Access:RW**
	Hilbert cfg pair-1	7:4	(bit[3:0] = Hilbert cfg pair-0)	
	Q0LP_SEL	3:2	low-pass filter alpha (=0: 1/256; =1: 1/1024; =2: 1/4096; =3: 1/16384)	
	Q0LP_EN	1	=1: reactive power 0 low-pass filter enable	
	HLBT0_EN	0	=1: hilbert filter 0 enable	
0x384D	**AFECFG3_B1**	**7:0**	**Default:0x00**	**Access:RW**
		7:4	Reserved	
	Hilbert cfg pair-2	3:0		
0x384E	**AFECFG3_B2**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	Reserved	
0x384F	**AFECFG3_B3**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	Reserved	
0x3850	**AFECFG4_B0**	**7:0**	**Default:0x00**	**Access:RW**
	DEC_SSEL	7:6	00: 0 01: 1 10: -2 11: -1	
		5	Reserved	
	EN_DC	4	=1: enable	
	EN_Integrator	3	=1: enable (only valid for I channel)	
	EM_HPF	2	=1: enable	
	EN_PWR_HPF	1	=1: enable	
	EN_SINC3	0	=1: enable	
0x3851	**AFECFG4_B1**	**7:0**	**Default:0x00**	**Access:RW**

AFE related Registers				
Addr	**Mnemonic**	**Bits**	**Description**	
	DEC_Phase	7:0	0~255, [SSEL, Phase] +/- 512	
0x3852	**AFECFG4_B2**	**7:0**	**Default:0x00**	**Access:RW**
	V channel 1	7:0	{AFECFG4_B1,AFECFG4_B0} is V channel0,this is V channel1 low byte	
0x3853	**AFECFG4_B3**	**7:0**	**Default:0x00**	**Access:RW**
	V channel 1	7:0	{AFECFG4_B1,AFECFG4_B0} is V channel0,this is V channel1 high byte	
0x3854	**AFECFG5_B0**	**7:0**	**Default:0x00**	**Access:RW**
	V channel 2	7:0	{AFECFG4_B1,AFECFG4_B0} is V channel0,this is V channel2 low byte	
0x3855	**AFECFG5_B1**	**7:0**	**Default:0x00**	**Access:RW**
	V channel 2	7:0	{AFECFG4_B1,AFECFG4_B0} is V channel0,this is V channel2 high byte	
0x3856	**AFECFG5_B2**	**7:0**	**Default:0x00**	**Access:RW**
	V channel 3	7:0	{AFECFG4_B1,AFECFG4_B0} is V channel0,this is V channel3 low byte	
0x3857	**AFECFG5_B3**	**7:0**	**Default:0x00**	**Access:RW**
	V channel 3	7:0	{AFECFG4_B1,AFECFG4_B0} is V channel0,this is V channel3 high byte	
0x3858	**AFECFG6_B0**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	AFE configuration register I0, I1	
0x3859	**AFECFG6_B1**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	AFE configuration register I0, I1	
0x385A	**AFECFG6_B2**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	AFE configuration register I0, I1	
0x385B	**AFECFG6_B3**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	AFE configuration register I0, I1	
0x385C	**AFECFG7_B0**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	AFE configuration register I2, I3	
0x385D	**AFECFG7_B1**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	AFE configuration register I2, I3	
0x385E	**AFECFG7_B2**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	AFE configuration register I2, I3	
0x385F	**AFECFG7_B3**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	AFE configuration register I2, I3	

Table 8-3：Analog Configuration Registers

Analog Configuration Registers				
Addr	**Mnemonic**	**Bits**	**Description**	
0x3860	**ICCFG0**	**7:0**	**Default:0x44**	**Access:RW**
		7:6	{DG_P03_DIS_C,DG_P03_DIS_PULLUP}	
		5:4	{DG_P02_DIS_C,DG_P02_DIS_PULLUP}	
		3:2	{DG_P01_DIS_C,DG_P01_DIS_PULLUP}	
		1:0	{DG_P00_DIS_C,DG_P00_DIS_PULLUP}	
0x3861	**ICCFG1**	**7:0**	**Default:0x45**	**Access:RW**
		7:6	{DG_P07_DIS_C,DG_P07_DIS_PULLUP}	
		5:4	{DG_P06_DIS_C,DG_P06_DIS_PULLUP}	
		3:2	{DG_P05_DIS_C,DG_P05_DIS_PULLUP}	
		1:0	{DG_P04_DIS_C,DG_P04_DIS_PULLUP}	
0x3862	**ICCFG2**	**7:0**	**Default:0x55**	**Access:RW**
		7:6	{DG_P11_DIS_C,DG_P11_DIS_PULLUP}	
		5:4	{DG_P10_DIS_C,DG_P10_DIS_PULLUP}	
		3:2	{DG_P09_DIS_C,DG_P09_DIS_PULLUP}	
		1:0	{DG_P08_DIS_C,DG_P08_DIS_PULLUP}	
0x3863	**ICCFG3**	**7:0**	**Default:0x52**	**Access:RW**
		7:6	Reserved	
		5:4	{DG_P14_DIS_C,DG_P14_DIS_PULLUP}	
		3:2	{DG_P13_DIS_C,DG_P13_DIS_PULLUP}	
		1:0	{DG_P12_DIS_C,DG_P12_DIS_PULLUP}	
0x3864	**ANA_KEY1**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	Write analog register must first hit the ANA_KEY1 & ANA_KEY2, ANA_KEY1 = 8'he4	
0x3865	**ANA_KEY2**	**7:0**	**Default:0x00**	**Access:RW**
		7:6	Write analog register must first hit the ANA_KEY1 & ANA_KEY2, ANA_KEY2 = 8'h1b	
0x3866	**DG_IO_3V**	**7:0**	**Default:0x8C**	**Access:RW**
	Extra Current sources	7:4	B[3:0]=0001，Current Strength=40uA B[3:0]=0010，Current Strength=80uA B[3:0]=0100，Current Strength=160uA B[3:0]=1000，Current Strength=320uA	
	XTAL power Down	3	1 : Active 0 : Power Down	
		2	0: weak pull up 1: strong pull up (180 ohm) ,rst_weak_phn	
		1	reset_pad disable pullup resistor (rst_dis_pullr)	
		0	reset pad disable input (rst_dis_c)	
0x3868	**DG_VREF_TR_3V**	**7:0**	**Default:0x00**	**Access:RW**
		7:0	Total 256 step from 1.2V to 1.32223V，VREF trimming resolution =0.435mV~0.528mV	
0x3869	**DG_BG_TR_3V**	**7:0**	**Default:0x00**	**Access:RW**

Analog Configuration Registers				
Addr	**Mnemonic**	**Bits**	**Description**	
		7	Reserved	
		6:0	Total 128 steps from 1198mV to 1236mV, resolution=302uV	
0x386A	**DG_PD_3V_B0**	**7:0**	**Default:0x00**	**Access:RW**
		7	WD_OSC power down	
		6:5	Reserved	
		4	LDOD power down	
		3	LDOA power down	
		2	PAD_VREFBUF power down	
		1	IBGEN_B power down	
		0	Bandgap power down	
0x386B	**DG_PD_3V_B1**	**7:0**	**Default:0x00**	**Access:RW**
		7	osc_por_control power down (controlled by hardware, not FW)	
		6:5	Reserved	
		4	set all AV18 domain register out to "0" from level shifter	
		3	set all AV18 power down pin to "1" from level shifter	
		2	set all AV18 domain register to "0" from level shifter	
		1	power down avdd3 power good	
		0	power down DG_VIND_PG	
0x386C	**DG_TST_3V_B0**	**7:0**	**Default:0x00**	**Access:RW**
		7	Reserved	
		6	1: wd_osc clock output to test pad	
		5:2	Reserved	
		1	IBGEN bandgap test voltage output 1: switch bangap voltage in/out from test pad	
		0	IBGEN bias test current output 1: switch tested bias current 20uA from power	
0x386D	**DG_TST_3V_B1**	**7:0**	**Default:0x00**	**Access:RW**
		7	1:PAD_TST ENABLE 0: PAD_TST DISABLE	
		6:3	Reserved	
		2	1: IADC TST(10uA)	
		1	Reserved	
		0	1:PAD_VREFBUF output to test pad	
0x386E	**DG_PD_B0**	**7:0**	**Default:0xFF**	**Access:RW**
	Adc_sdm(IB)	7	ADC power down [7] vmid	
	Adc_sdm(IA)	6:0	ADC power down [0] vmid [1] adc_clkgen [2] pga [3] modulator [4] adc_mod_im	

Analog Configuration Registers				
Addr	**Mnemonic**	**Bits**	**Description**	
			[5] ain0 adc_sd_inbuf [6] ain1 adc_sd_inbuf	
0x386F	**DG_PD_B1**	**7:0**	**Default:0xBF**	**Access:RW**
		7	TSENSOR power down	
		6	1: 16MHz RC oscillator power down , 0: power on	
	Adc_sdm(IB)	5:0	ADC power down [0] adc_clkgen [1] pga [2] modulator [3] adc_mod_im [4] ain0 adc_sd_inbuf [5] ain1 adc_sd_inbuf	
0x3870	**DG_REG_B0**	**7:0**	**Default:0x00**	**Access:RW**
		7:6	{DG_REG_B1[0], DG_REG_B0[7:6]} IA channel decoder for input setting 000 : adc wth input buffer 001 : adc wth input buffer 010 : adc unity input buffer 011 : adc unity input buffer 100 : PAD_VREF 101 : LDOA 110 : AVSS 111 : AVSS	
		5:3	IB channel gain setting 000 : x1 , 001 : x2 , 010 : x4 , 011 : x8 , 100 : x16 , 101 : x24 110 : x32 , 111 : Input short to VGND	
		2:0	IA channel gain setting 000 : x1 , 001 : x2 , 010 : x4 , 011 : x8 , 100 : x16 , 101 : x24 110 : x32 , 111 : Input short to VGND	
0x3871	**DG_REG_B1**	**7:0**	**Default:0x50**	**Access:RW**
	bias current trimming for SDM ADC IA	7:5	IA PGA bias current 000 : 1uA , 001 : 1.5uA , 010 : 2uA , 011 : 2.5uA, 100 : 3uA , 101 : 3.5uA , 110 : 4uA , 111 : 4.5uA	
	bias current trimming for SDM ADC IA	4	IA input buffer bias current 0 : 1uA , 1 : 2uA	
		3:1	IB channel decoder for input setting 000 : adc wth input buffer 001 : adc wth input buffer 010 : adc unity input buffer 011 : adc unity input buffer 100 : LDOD 101 : TEMP 110 : AVSS	

Analog Configuration Registers				
Addr	**Mnemonic**	**Bits**	**Description**	
			111 : AVSS	
		0	With DG_REG_B0[7:6]	
0x3872	**DG_REG_B2**	**7:0**	**Default:0x55**	**Access:RW**
	bias current trimming for SDM ADC IB	7:6	IB Modulator bias current 00 : 0.5uA , 01 : 1uA , 10 : 1.5uA , 11 : 2uA	
	bias current trimming for SDM ADC IB	5:3	IB PGA bias current 000 : 1uA , 001 : 1.5uA , 010 : 2uA , 011 : 2.5uA, 100 : 3uA , 101 : 3.5uA , 110 : 4uA , 111 : 4.5uA	
	bias current trimming for SDM ADC IB	2	IB input buffer bias current 0 : 1uA , 1 : 2uA	
	bias current trimming for SDM ADC IA	1:0	IA Modulator bias current 00 : 0.5uA , 01 : 1uA , 10 : 1.5uA , 11 : 2uA	
0x3873	**DG_REG_B3**	**7:0**	**Default:0x03**	**Access:RW**
		7:6	Reserved	
		5	1:enhance vmid_mod driving capability	
		4	1:enhance vmid_pga driving capability	
		3	IB en_chop 0: disable chopping 1: enable chopping	
		2	IA en_chop 0: disable chopping 1: enable chopping	
		1	IB ADC resetn , 0:resetn	
		0	IA ADC resetn , 0:resetn	
0x3874	**DG_REG_B4**	**7:0**	**Default:0x00**	**Access:RW**
		7	TSENSOR test voltage output 0: delta VBE curve 1: single VBE curve (save power, large voltage)	
		6	Reserved	
		5	1 : IB ADC input=0	
		4	1 : IA ADC input=0	
		3:2	Reserved	
		1	1:enhance vmid_mod driving capability	
		0	1:enhance vmid_pga driving capability	
0x3875	**DG_REG_3V_B0**	**7:0**	**Default:0x56**	**Access:RW**
		7:6	IB control for IB[1], wt_osc bias current 00:0.5uA/ 01:1uA/ 10:2uA/ 11: 4uA	
		5:4	IB control for IB[0], tsensor bias current 00:0.5uA/ 01:1uA/ 10:2uA/ 11:4uA	
		3:1	ADC Bias Current Setting IADC[2:0] | 000:0.5uA /001:1uA /010:1.5uA /011:2uA /100:2.5uA /101:3uA /110:3.5uA /111:4uA Default:2uA	
		0	Reserved	
0x3876	**DG_REG_3V_B1**	**7:0**	**Default:0x02**	**Access:RW**
		7:6	Digital Core LDO with external 0.1uF | 00:1.8V / 01:1.7V /10:1.6V /11:1.9V	

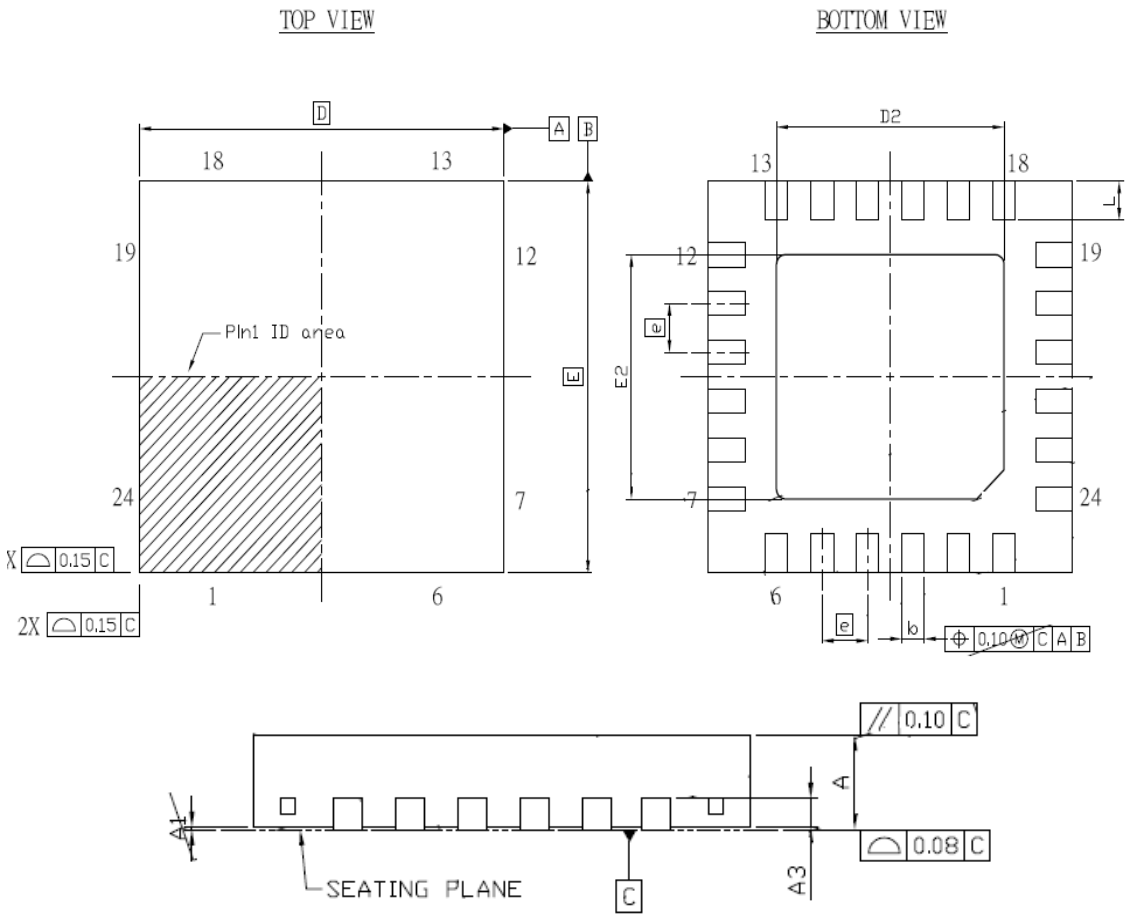
Analog Configuration Registers			
Addr	**Mnemonic**	**Bits**	**Description**
		5:4	Analog Core LDO with external 0.1uF | 00:1.8V / 01:1.7V /10:1.6V /11:1.9V
		3:2	Reserved
		1:0	IB control for IB[2], VREF_BUF bias current 00:0.5uA/ 01:1uA/ 10:2uA/ 11: 4uA
0x3877	**DG_REG_3V_B2**	**7:0**	**Default:0x40** **Access:RW**
	coarse frequency adjustment	7	{DG_REG_3V_B3[0],DG_REG_3V_B2[7]}
	fine frequency adjustment from 200KHz to 700KHz	6:0	1000000 : default value. No frequency shift from coarse frequency 0010001 : shift - 5 KHz from coarse frequency 0010000 : -10 KHz 0100111 : -15 KHz 0100110 : -20 KHz 0110111 : -25 KHz 0110110 : -30 KHz 0100101 : -35 KHz 0100100 : -40 KHz 0110101 : -45 KHz 0110100 : -50 KHz 0100011 : -55 KHz 0100010 : -60 KHz 0110010 : -70 KHz 0100000 : -80 KHz 0110000 : -90 KHz : : 1110000 : -170 KHz 0000001 : shift + 5 KHz from coarse frequency 0010010 : +10 KHz 0010011 : +15 KHz 0000010 : +20 KHz 0000011 : +25 KHz 0010100 : +30 KHz 0010101 : +35 KHz 0000100 : +40 KHz 0010110 : +50 KHz 0000110 : +60 KHz 0011000 : +70 KHz 0001000 : +80 KHz 0011010 : +90 KHz 0001010 : +100 KHz : : 0001111 : +145 KHz

Analog Configuration Registers				
Addr	**Mnemonic**	**Bits**	**Description**	
0x3878	**DG_REG_3V_B3**	**7:0**	**Default:0x10**	**Access:RW**
	4 bits to NT trimming temperature coefficient	7:5	{DG_REG_3V_B4[0],DG_REG3V_B3[7:5]}	
	4 bits to PT trimming temperature coefficient	4:1	Positive Temperature Coefficient	
	coarse frequency adjustment	0	00 : 20.8KHz 01 : 32.3KHz 10 : 91.6KHz 11 : 500KHz	
0x3879	**DG_REG_3V_B4**	**7:0**	**Default:0x03**	**Access:RW**
		7:3	Reserved	
	WD Trig Signal	2	1 : Initialization 0 : Active	
	WD Bias Current Select	1	1:Internal Bias 0:External Bias	
	4 bits to NT trimming temperature coefficient	0	Negative Temperature Coefficient	
0x387B	**DG_OSC_B0**	**7:0**	**Default:0xBE**	**Access:RW**
	Negative Temperature Coefficient Current Tuning	7:6	{DG_OSC_B1[3:0],DG_OSC_B0[7:6]}	
	Positive Temperature Coefficient Current Tuning	5:0	Output Current=0.5uA	
0x387C	**DG_OSC_B1**	**7:0**	**Default:0x8F**	**Access:RW**
	Bias Current Tuning	7:4	{DG_OSC_B2[0],DG_OSC_B1[7:4]	
	Negative Temperature Coefficient Current Tuning	3:0	Output Current=0.5uA	
0x387D	**DG_OSC_B2**	**7:0**	**Default:0x28**	**Access:RW**
	Charge/Discharge Current Tuning	7:6	{DG_OSC_B3[4:0],DG_OSC_B2[7:6]}	
	Reference Voltage	5:1	VREF=0.6V	

Analog Configuration Registers			
Addr	**Mnemonic**	**Bits**	**Description**
	Tuning		
	Bias Current Tuning	0	Output Current=0.25uA Bias Current =PT Current +NT Current
0x387E	**DG_OSC_B3**	**7:0**	**Default:0x09** **Access:RW**
	High Current Mode Current Tuning	7	{DG_OSC_B4[1:0],DG_OSC_B3[7]}
	Test Mode	6:5	B[1:0]=00 No Test Signal Out B[1:0]=01 VREF B[1:0]=10 20uA B[1:0]=11 N/C
	Charge/Discharge Current Tuning	4:0	Charge/Discharge Current=0.5uA
0x387F	**DG_OSC_B4**	**7:0**	**Default:0x02** **Access:RW**
		7:2	Reserved
	High Current Mode Current Tuning	1:0	Output Current=0.5uA

9. Package Outline Dimension

9.1 24-Pin QFN Package (4x4)



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.5	29.5	31.5
A1	0	0.02	0.05	0	0.79	1.97
A3	0.203 REF			8 REF		
b	0.18	0.25	0.30	7.1	9.8	11.8
D	3.90	4.00	4.10	153.5	157.5	161.4
D2	2.40	2.50	2.60	94.5	98.4	102.4
E	3.90	4.00	4.10	153.5	157.5	161.4
E2	2.40	2.50	2.60	94.5	98.4	102.4
e	0.50 BSC			19.7 BSC		
L	0.30	0.40	0.50	11.8	15.7	19.7

Figure 9-1: PL7413 Package Outline Diagram (QFN24 4x4)

10. ORDERING INFORMATION

Table 10-1：Ordering Information

Model/Device	Package Type	Pins	Package Qty	Prolific Type Code	ECO
PL7413	QFN	24	4000pcs / Reel	PL7413C1FIG8P1	Green (RoHS)
PL7413	QFN	24	4900pcs / Tray	PL7413C1FIG7P1	Green (RoHS)

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