2-Channel Power/Energy Metering Analog Front End (AFE)

Product Datasheet PL7211

Features

- 2-Channel 24-bit sigma-delta ADC
- Internal 3.3V/5V to 1.8V cap-less LDO
- Internal 1.2V cap-less VREF (w/ 0.1% accuracy/full temp. range after trim)
- Built-in 1X ~ 32X PGA (w/ 0.1% accuracy/full temp. range after calibration)
- Internal 16MHz RC OSC (w/ 0.2% accuracy/full temp. range after trim)
- Internal VDT/POR and temperature sensor
- Built-in FIR filter for each individual channel
- Channel phase alignment
- Programmable 48-bit DSP engine with
  - 512 x 32 program space
  - 128 x 48 data space
  - 64 x 48 output buffer
  - Built-in fix point to float-point converter
- 8KB OTP with 2 banks DSP code, DSP CFG and SYS CFG
- Supports I2C/SPI/UART (UART supports auto baud-rate mode)
- Supports 38KHz IR carrier removed
- Supports up to 9 GPIOs which can be directly controlled by DSP
- 5V tolerance I/O
- Small package size: 4x4 QFN24

Typical Applications

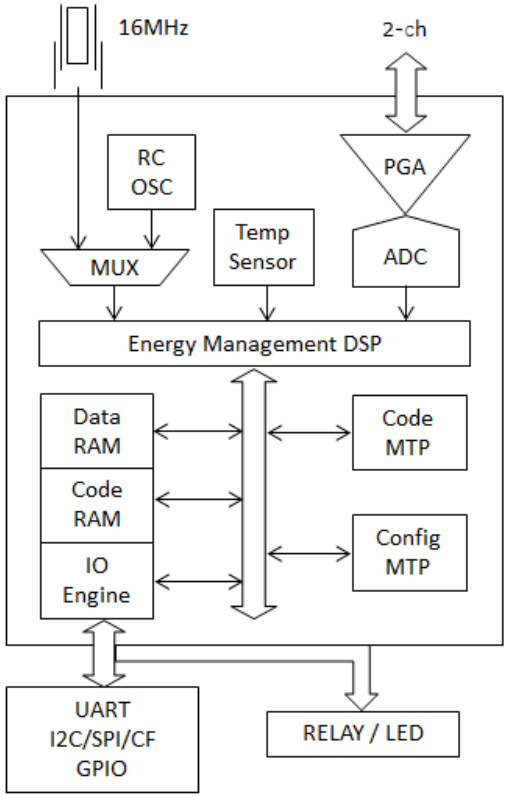
- Smart Plug/Strip/PDU
- Protection Device/Home Appliance
- Power Monitor, Hardware Monitor

General Description

The PL7211 is a highly integrated power/energy monitoring Analog Front End (AFE) IC that measures electricity-related data for power usage measurement applications. It has built-in 8-channel ADC and a programmable DSP which can adapt to different applications such as metering, power protection and Master/Slave.

The PL7211 has a built-in MTP that stores the chip configuration, DSP code and calibration data. It provides SPI slave interface and can be used for calibration and programming data or DSP code. MCU can be accessed through SPI interface.

The PL7211 can diagnose the electricity-related data to identify overloading, short circuit, leakage current and arcing condition for further power protection features. It also provides a flexible architecture, low system BOM cost and programmable solution, to help manufacturers minimize development efforts and design a versatile and flexible product.



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Block Diagram

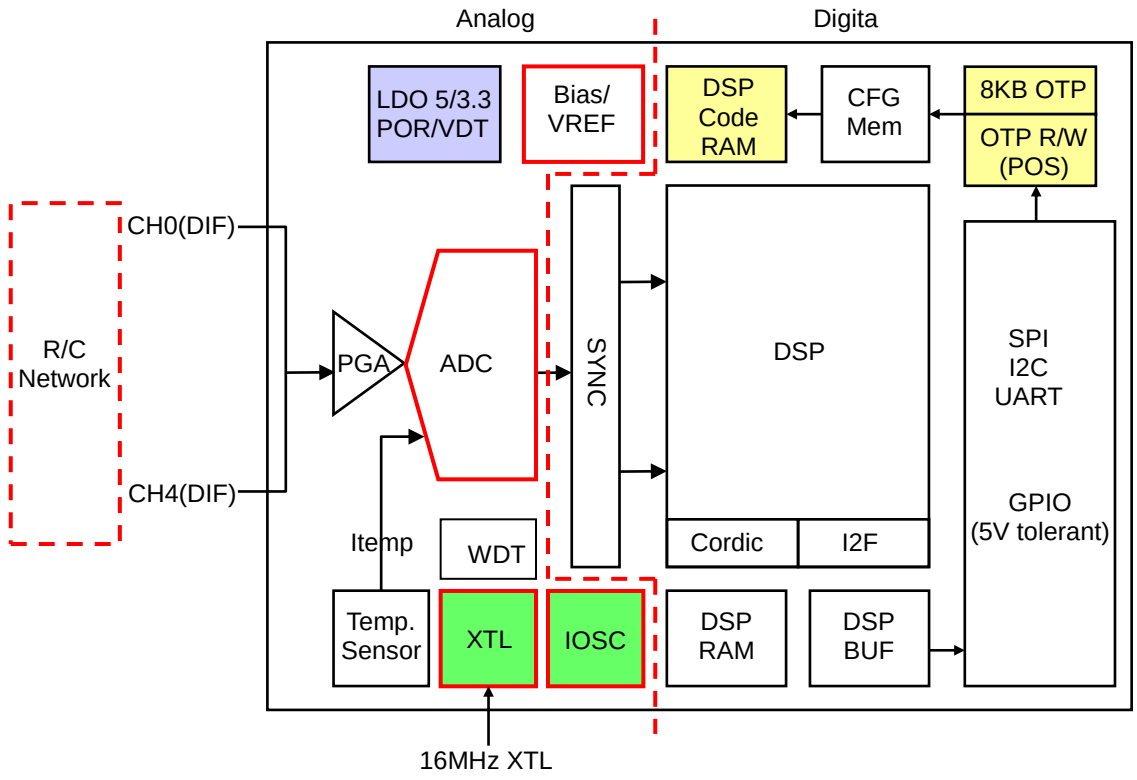


Figure 1-1: Function Block Diagram

Table of Contents

List of Figures

List of Tables

1. Detailed Features

1.1 General Features

- 2-Channel 24-bit sigma-delta ADC
- 3V to 5V wide range power supply with 5V-tolerant I/O
- H/W DSP for power parameter calculation
- DSP Code upgradeable by MCU
- Low power consumption
  - 4.6mA@3.3V, full operation
  - 2.3mA@3.3V, low power mode
- Operation temperature range: -20 °C to +85 °C
- Small package size: 4x4 QFN24

1.2 ADC

- 24-bit ADC with PGA
- PGA Gain 1X ~ 32X
- 2-Channel individual decimator
- Built-in internal 1.2V VREF for ADC measurement
- VREF accuracy is +/- 0.2%
- Channel data phase aligner
- Built-in FIR filter for each channel

1.3 DSP

- Programmable 48-bit DSP engine with
  - 512 x 32 program space
  - 128 x 48 data space
  - 64 x 48 output buffer
- 8KB OTP with 2 banks DSP code, DSP CFG and SYS CFG
- Supports RMS, active power, reactive power, apparent power, Power factor, KWH calculation
- SAG/SWELL, Over-Current, Over-Watt, Leakage Protection
- THD/Harmonic Calculation
- Supports AC/DC measurement (possible to dynamic adjust by MCU)
- Built-in fix-point to IEEE 754 floating point format converter

1.4 Clock System

- Supports up to 16MHz external crystal input
- Built-in internal 16MHz +/- 5% OSC
- Anti-fail clock auto switch
- System clock divider for each block
- Built-in internal watch-dog timer with IO interrupt output

1.5 SPI Interface

- SPI Slave mode supports mode 0, mode 1, mode 2, and mode 3
- Supports single and multi-byte read/write
- Supports CRC data check

1.6 I2C Interface

- I2C interface
- Two hardware slave ID selection for cascade application
- Software ID programmable
- Supports single and multi-byte read/write
- Supports CRC data check

1.7 UART

- Auto baud-rate learning
- Two hardware slave ID selection for cascade application
- Software ID programmable
- Supports single and multi-byte read/write
- Supports CRC data check
- Supports UART timeout
- Supports IR 38KHz carrier removed
- UART master mode for auto data report

1.8 GPIO

- Programmable IN/OUT control
- Selectable control by DSP or register setting
- 5V tolerance

2. Pin Out Diagram and Description

2.1 24-Pin QFN Pin Diagram

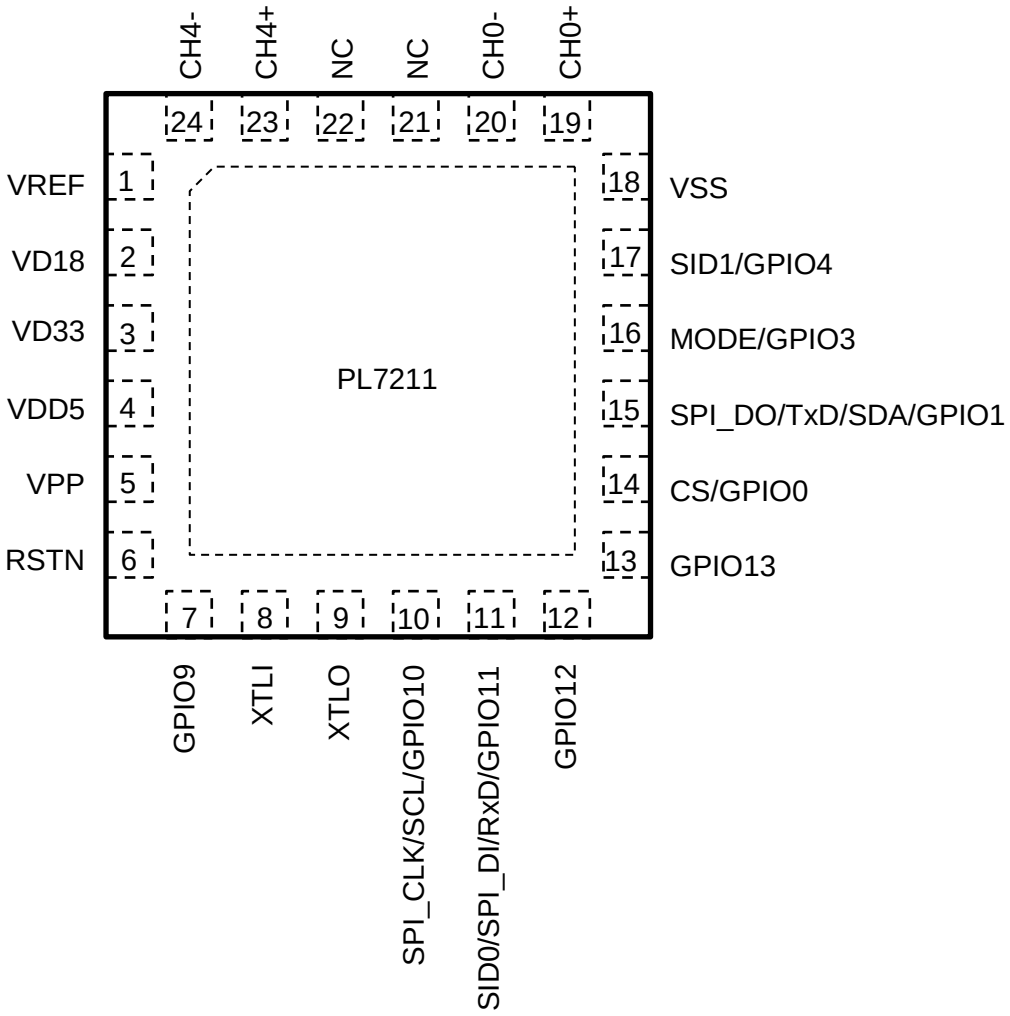


Figure 2-1: PL7211 Pin Diagram (QFN24)

2.2 24-Pin QFN Pin-Out Description

Table 2-1：PL7211 QFN24 Pin Name Table

Pin #	Pin Name	Type	Pin Description
1	VREF	Analog output	Internal voltage reference
2	VD18	Power	1.8V LDO output (Analog)
3	VD33	Power	VDD33 output
4	VDD5	Power	5V power input
5	VPP	Power	OTP 6.5V programming power input
6	RSTN	Digital Input/Output	Reset input (active low)
7	GPIO9	Digital Input/Output	GPIO9
8	XTLI	Crystal Input	16MHz Crystal input pad
9	XTLO	Crystal Output	16MHz Crystal output pad
10	SP_CLK/SCL/GPIO10	Digital Input/Output	Multi-function IO, GPIO#10
11	SID0/SPI_DI/RxD/ GPIO11	Digital Input/Output	Multi-function IO, GPIO#11
12	GPIO12	Digital Input/Output	GPIO12
13	GPIO13	Digital Input/Output	GPIO13
14	CS/GPIO0	Digital Input/Output	Multi-function IO, GPIO0
15	SPI_DO/TxD/SDA/GPIO1	Digital Input/Output	Multi-function IO, GPIO1
16	MODE/GPIO3	Digital Input/Output	Multi-function IO, GPIO3
17	SID1/GPIO4	Digital Input/Output	Multi-function IO, GPIO4
18	VSS	Ground	Digital Ground
19	CH0+	Analog Input	Analog CH0 differential input +
20	CH0-	Analog Input	Analog CH0 differential input -
21	NC	-	No Connection
22	NC	-	No Connection
23	CH4+	Analog Input	Analog CH4 differential input +
24	CH4-	Analog Input	Analog CH4 differential input -

3. Electrical Characteristic

3.1 Absolute Maximum Rating

Table 3-1：Absolute Maximum Rating

Parameter	Max Value
VDD5	6V
AVDD3	4.0V
DVDD3	4.0V
Analog input	-0.5V ~ +0.5V
Digital I/O input	-0.3V ~ AVDD + 0.3V
Input Current (Digital IO)	20uA
Output Current (IO Pin)	6mA
Operation Temperature	-20°C ~ 85°C
Storage Temperature	-40°C ~ 150°C
ESD	4KV(HBM)/500V(MM)

3.2 Recommended Operation Conditions

Table 3-2：Recommended Operation Conditions

Parameter	Max Value
VDD5	4.5V ~ 5.5V
AVDD3	3.0V ~ 3.3V
DVDD3	3.0V ~ 3.3V
VPP	6.5
Analog input	-0.3V ~ 0.3V
XTL	16MHz

3.3 AC/DC Characteristics

Table 3-3：AC/DC Characteristics

(All parameters apply at VDD=3.3 V±10%, AGND=DGND=0 V, Internal Reference, XTAL=8MHz, TMIN to TMAX = - 20°C to +85°C.)

Parameters	Test Condition	Min.	Typ.	Max.	Units
VAIN	ADC input (differential)	-0.45		0.45	V
	ADC Single-end w buffer	0.2		0.9	V
	ADC Single-end wo buffer	-0.45		0.45	V
PGA	Gain 1X, 2X, 4X, 8X, 16X, 32X				
VADC	PGA=1X	-320		320	mV
	PGA=2X	-160		160	mV

	PGA=4X	-80		80	mV
	PGA=8X	-40		40	mV
	PGA=16X	-20		20	mV
	PGA=32X	-10		10	mV
ADC	Data output		24		Bits
	Data range	-2^22		2^22	
	OSR selection: 64/128/256				
	Latency selection	4		7	
	ADC noise free bits		14.5		Bits
ODR	ADC output data rate (depends on channel mux setting)			1600	SPS
OSC					
Fosc	Internal OSC frequency		16		MHz
Icc_osc					uA
	Trimming step		20		KHz
	Internal OSC stability (-20~85C)				%
XTL PAD			16		MHz
	Duty cycle		50		%
	Crystal start-up time				us
IO PAD					
VIH		2.3			V
VIL				1	V
VOH		3.0			V
VOL				0.3	V
	I2C speed@16MHz		400		KHz
	SPI speed@16MHz		2		MHz
	UART baud rate@16MHz		115		KHz
Power Consumption					
Icc	2 LED / 2 ambient 200 samples second				mA
	2 LED / 2 ambient 100 samples second				mA
	2 LED / 2 ambient 50 samples second				mA

4. Function Description

4.1 AFE (Analog Front-End)

The PL7211 can work as an AFE (Analog Front-End) with SPI interface. It can measure the V/I real-time data, V/I rms, Watt, VA, PF, and line frequency. Users can utilize this information for further energy management. The following table depicts the parameters that can be accessed through the PL7211 SPI interface.

Table 4-1：AFE Measurement Parameters

Parameter	Description
V_{RMS}	RMS value of voltage
I_{RMS}	RMS value of current
Power	Active power value
PF	Power Factor
Frequency	Line Frequency

4.2 Power Protection

The power protection function of PL7211 prevents overload condition that may cause equipment to overheat or catch fire. When the load current exceeds the rated current (or pre-configured current threshold, $I_{LT/ST}$) for a specified time, the relay will be switched off to prevent overheat condition. Both the overload threshold current and delay time to switch off relay can be configured through the software provided by Prolific.

4.2.1 Power Protection Operation

The power protection operation is shown in Figure 4-1 and Figure 4-2:

- If the load current (I_{LOAD}) is less than or equal to $I_{LT/ST}$, the relay is always ON.
- If the load current (I_{LOAD}) is larger than $I_{LT/ST}$, the delay time (T_{OFF}) to switch off relay will be shorter. Refer to section 4.2.2 to calculate (T_{OFF}).
- Both the $I_{LT/ST}$ and $T_{LT/ST}$ can be configured by the application software provided by Prolific.

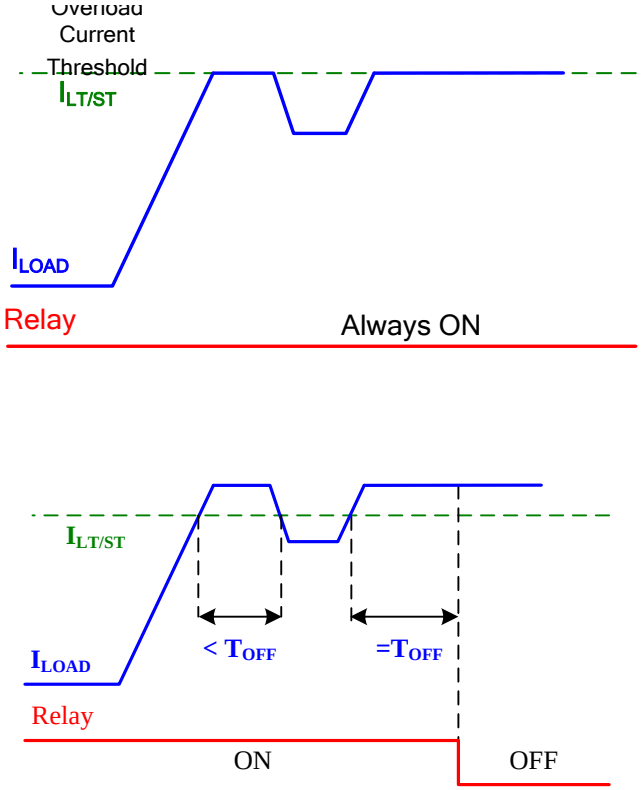


Figure 4-1: Description of long/short time protection (I_{LOAD} > $I_{LS/ST}$)

4.2.2 Delay Time to switch off relay

The delay time, T_{OFF}, can be calculated by the following equation:

$$T_{OFF} = T_{LT/ST} \times \left(\frac{I_{LT/ST}}{I_{LOAD}} \right)^2$$

For example,

- Short time threshold current (I_{ST}) is set as 30A
- T_{ST} is set as 5sec
- Exact load current is 50A.

The delay time to switch off relay is:

$$T_{OFF} = 5 \times \left(30 / 50 \right)^2 = 1.8 \text{sec}$$

5. Interface

➢ **IO Mode Selection**

IO Mode is latched when resetn is from low to high.

- i2c_en = [MODE pin, CS pin]= 2'b00
- uart_en = [MODE pin, CS pin]= 2'b01
- spi_en = [MODE pin, CS pin]= 2'b10
- gpio_en = [MODE pin, CS pin]= 2'b11

5.1 SPI Interface

The SPI bus is the interface to access internal memory/register/energy information of PL7211. The SPI interface of PL7211 is operated at slave mode; consequently, the external SPI device should serve as the SPI master. As shown in below diagram, the external SPI master sends Chip Select and Clock signal to SPI slave of PL7211. Data is written through SPI_DI and read through SPI_DO.

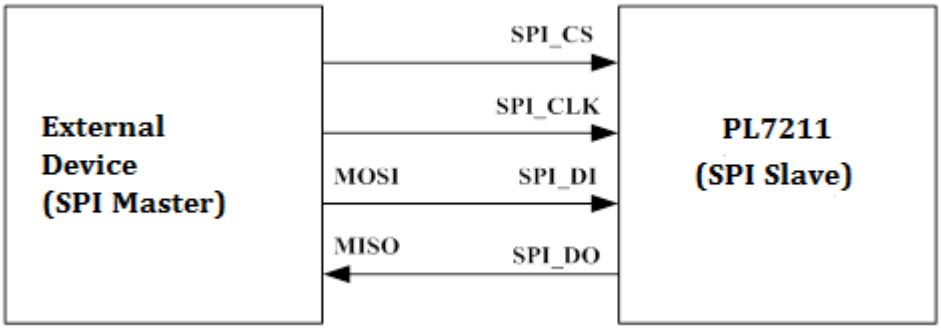


Figure 5-1: Connection scheme of SPI interface

5.1.1 SPI Command

➢ **spi_cmd[7]:** inc_adr_dis 1: disable address increment

Ex: checking whether dsp is ready. The address can be fixed.

dsp_status(cfg addr = 0x390a).

If DSPRDY is from 0 to 1, then master can read out dsp outbuffer data.

➢ **spi_cmd[6:4]:** read/write command

- spi_cmd[6:4] = 3'h1 for read with crc enable
- spi_cmd[6:4] = 3'h2 for write with crc enable
- spi_cmd[6:4] = 3'h3 for read with crc disable
- spi_cmd[6:4] = 3'h4 for write with crc disable

- **spi_cmd[3:0]:** Read/Write package number
  - case1: crc enable, set to 4, master must send out 4byte data + 1byte crc. Then slave will send out internal crc value to master.
  - case2: crc disable, set to 4, master must send out 4byte data. Then slave will not send out internal crc value to master.

5.1.2 SPI Mode

Default SPI is at mode3 and can be changed at power on sequence (OTP value).

- *spi_con = 0x3837(Must write the setting in OTP-CFG Bank0 at the start).*
  - Bit7 = cpol, clock polarity
  - Bit6 = cpha, clock phase
  - Bit5 = spr1, to select spi master clk
  - Bit4 = spr0, to select spi master clk
  - Bit3~0: no use
  - SPI master clk = fclk/2 (00), fclk/4(01), fclk/8(10), fclk/16(11)

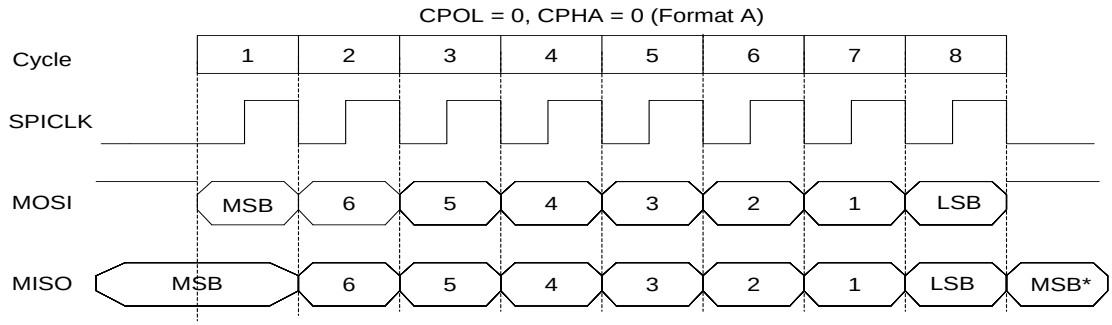


Figure 5-2(a): SPI Transfer Format

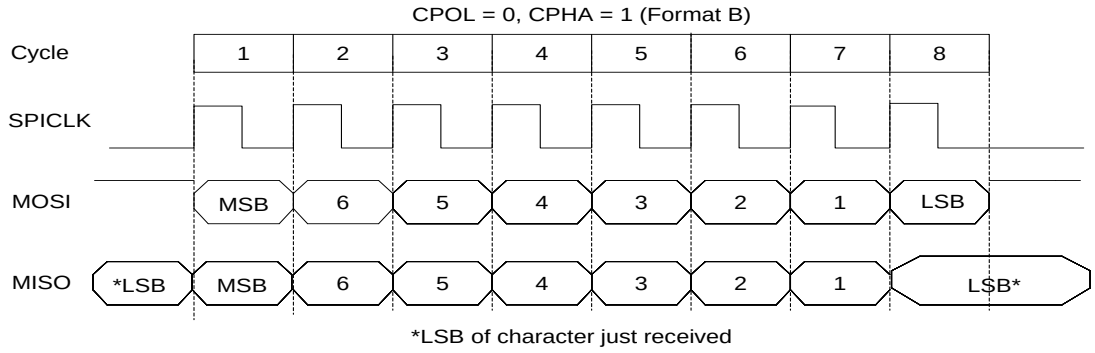


Figure 5-3(b): SPI Transfer Format

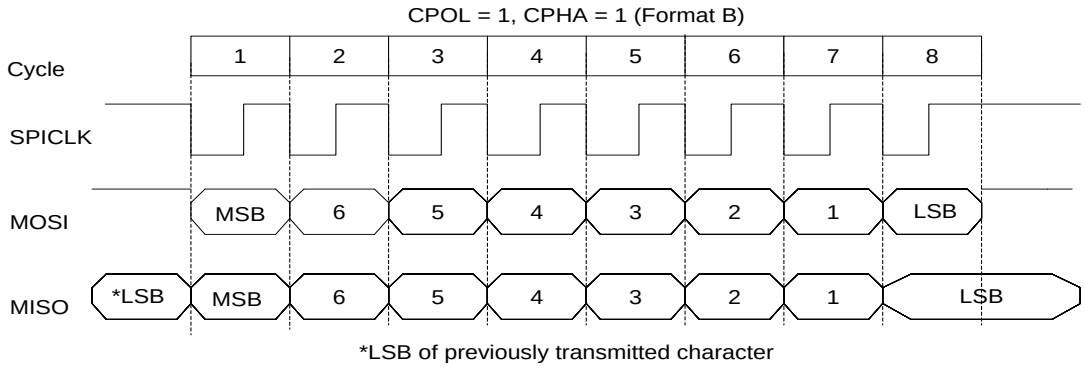


Figure 5-4(c): SPI Transfer Format

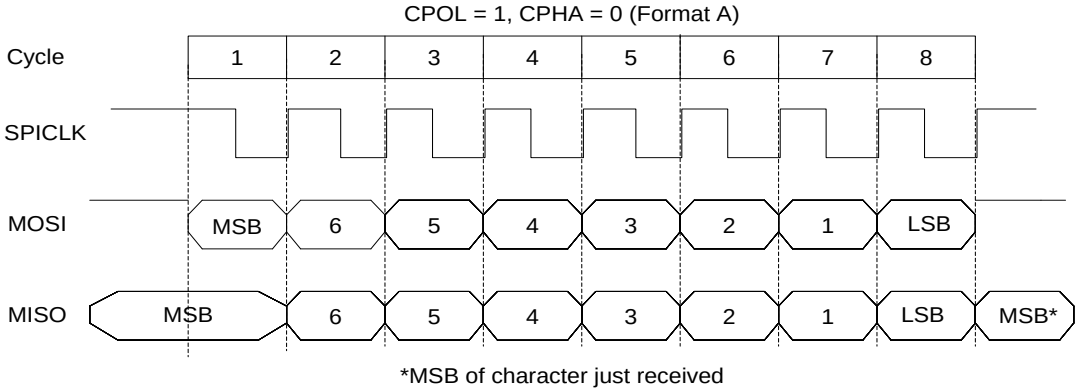


Figure 5-5(d): SPI Transfer Format

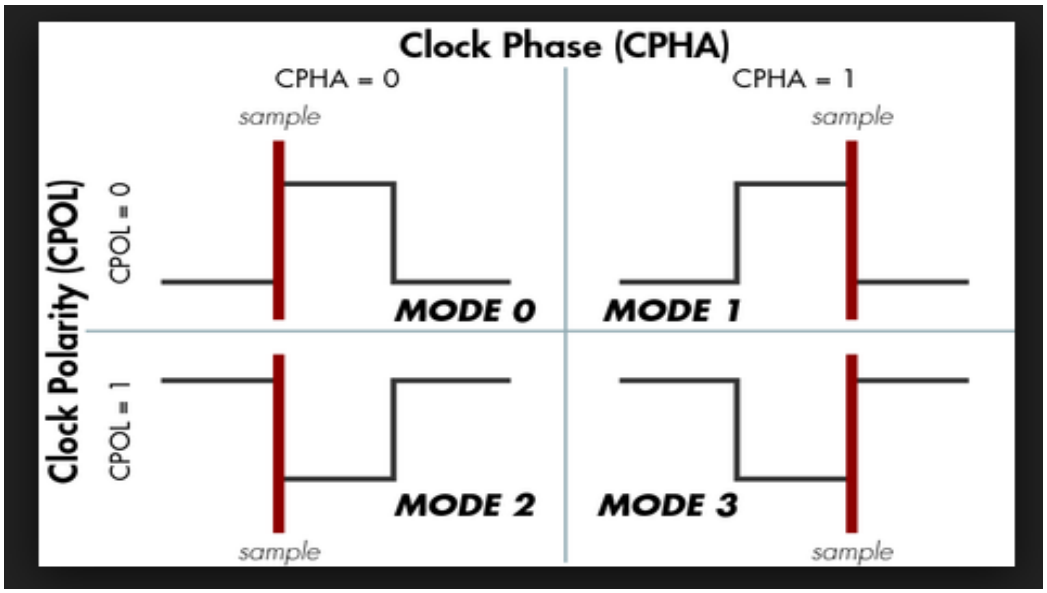


Figure 5-6: SPI Mode

- When length = 0, then hardware (IC) will set the internal length equal to d'96 so fw can read the data of dsp outbuf by 4 times (96*4 = 384 bytes) with crc.
- When crc is disabled, the length setting is ignored, and the state machine is left when spi_cs is from 0 to 1.
- If master crc is not the same as slave crc, then slave will go to error state, master must control spi_cs from 0 to 1 to let slave leave error state to idle state.
- When write to OTP memory, master must wait OTP is ready(0x80), then can continue writing the next byte.

5.1.3 SPI Timing

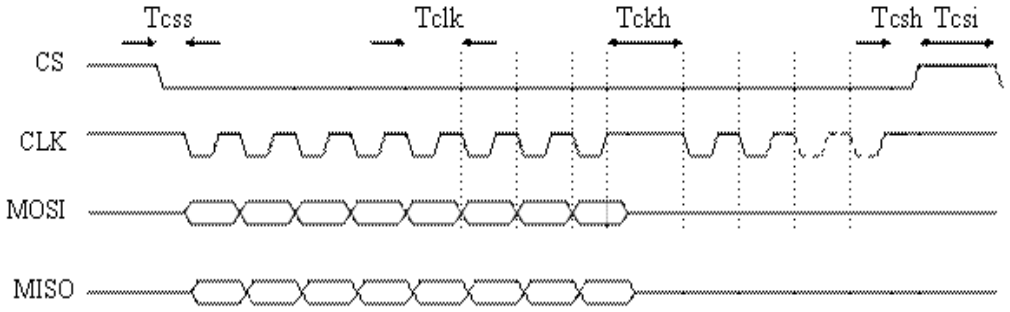


Figure 5-4: SPI Timing

- Tcss >= 3 system clk
- Tcsh >= 3 system clk
- Tcsi >= 3 system clk
- Tckh >= 1.5 spi_clk (about 1.5x4 = 6 system clk) for ram, cfg, buf.
- Tclk >= 4 system clk
- Tckh for OTP

  The first data output of OTP IP needs to be larger than 300ns. So when reading OTP, the Tckh, after finishing to send ADDRL, must be larger than (1.5 spi_clk + 300ns).

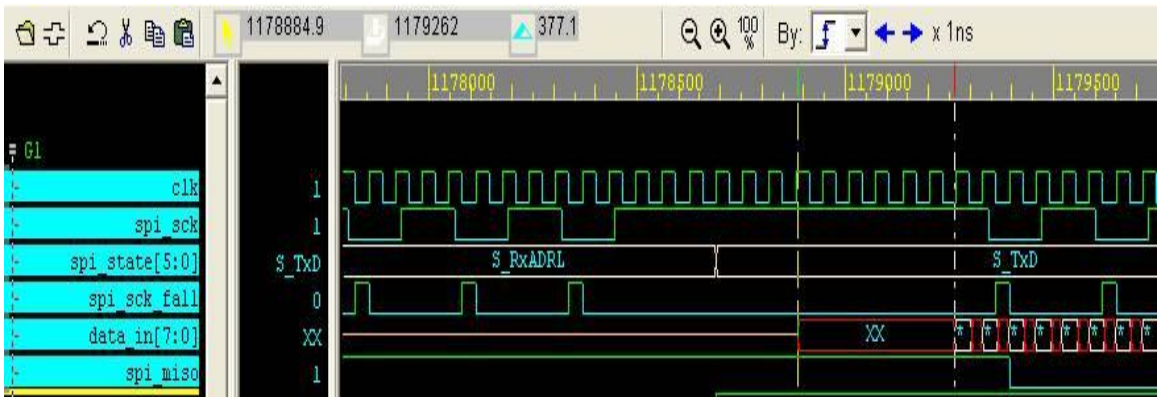


Figure 5-5: Tckh for OTP

5.1.4 SPI with CRC

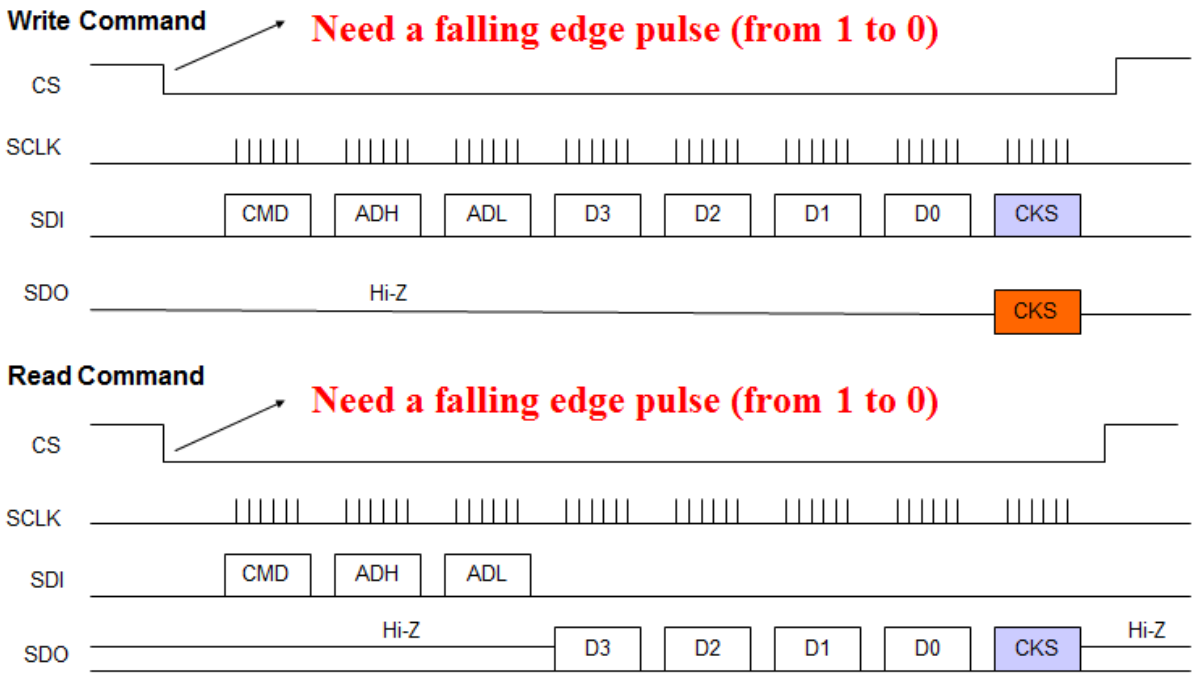


Figure 5-6: SPI with CRC

5.1.5 SPI without CRC

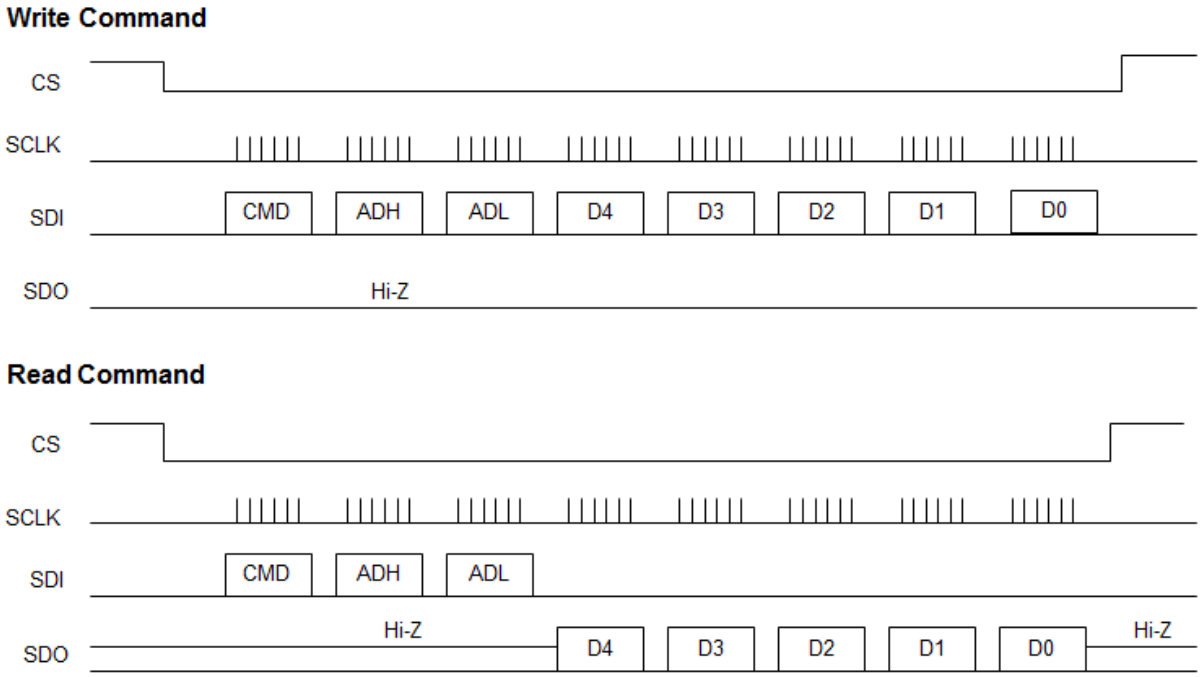


Figure 5-7: SPI without CRC

5.1.6 SPI OTP one byte with CRC

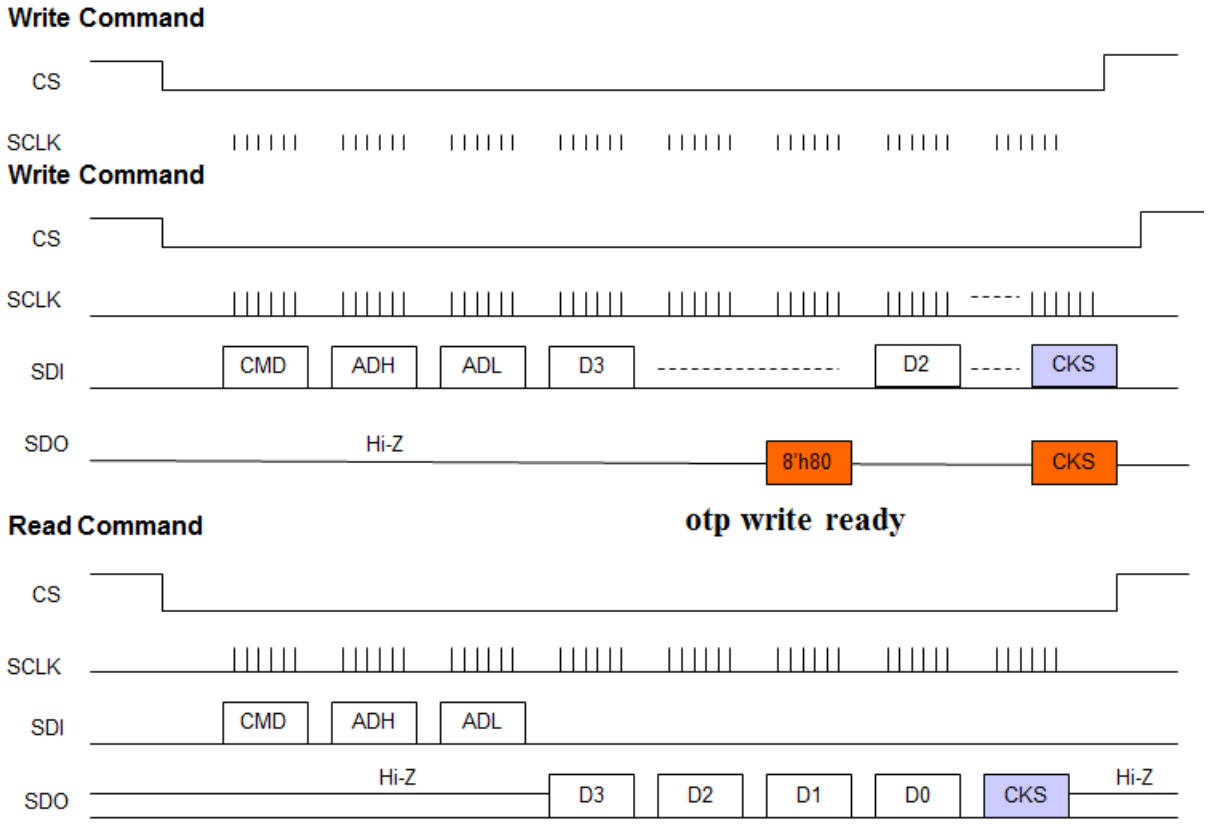


Figure 5-8: SPI OTP one byte with CRC

5.2 I2C Interface

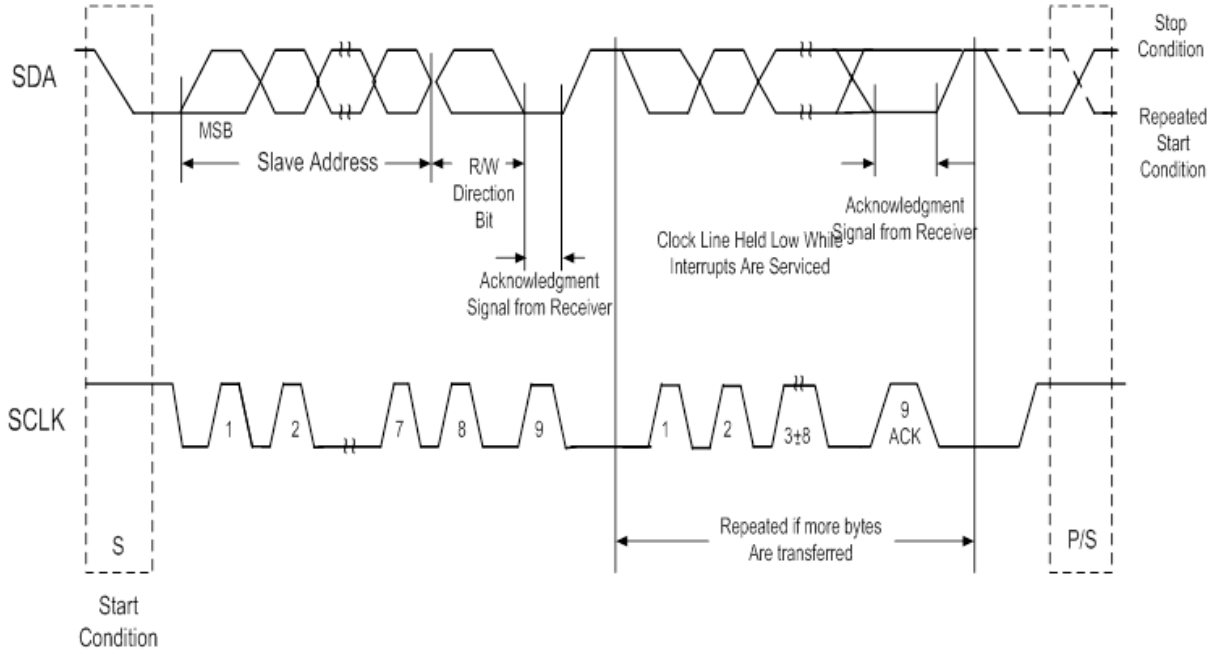


Figure 5-9: Waveform of I2C

5.2.1 I2C Write Sequence

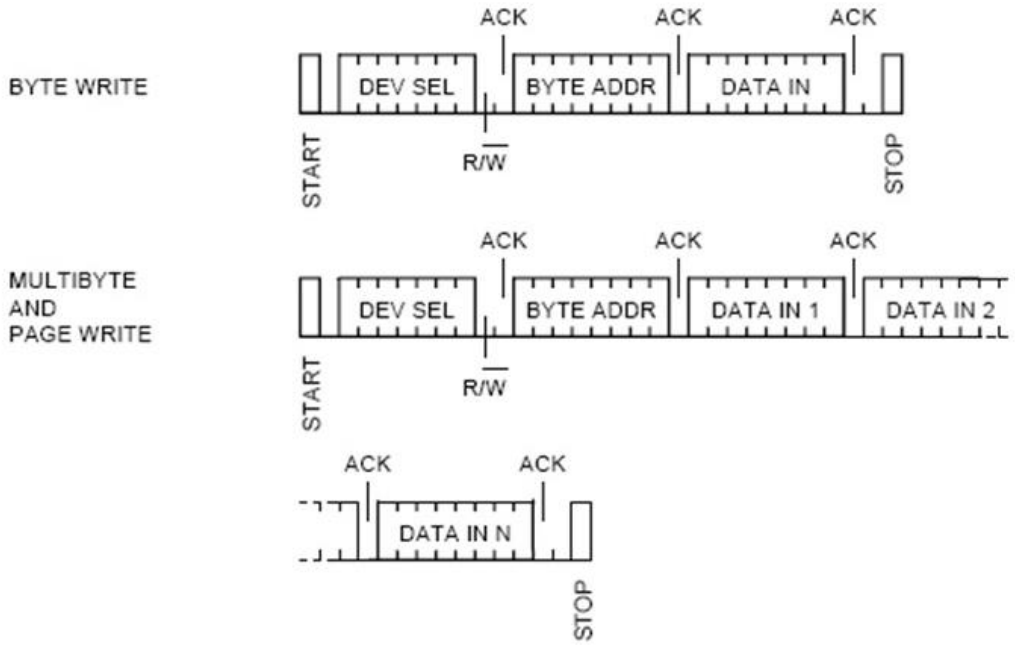


Figure 5-10: I2C Write Sequence (1)

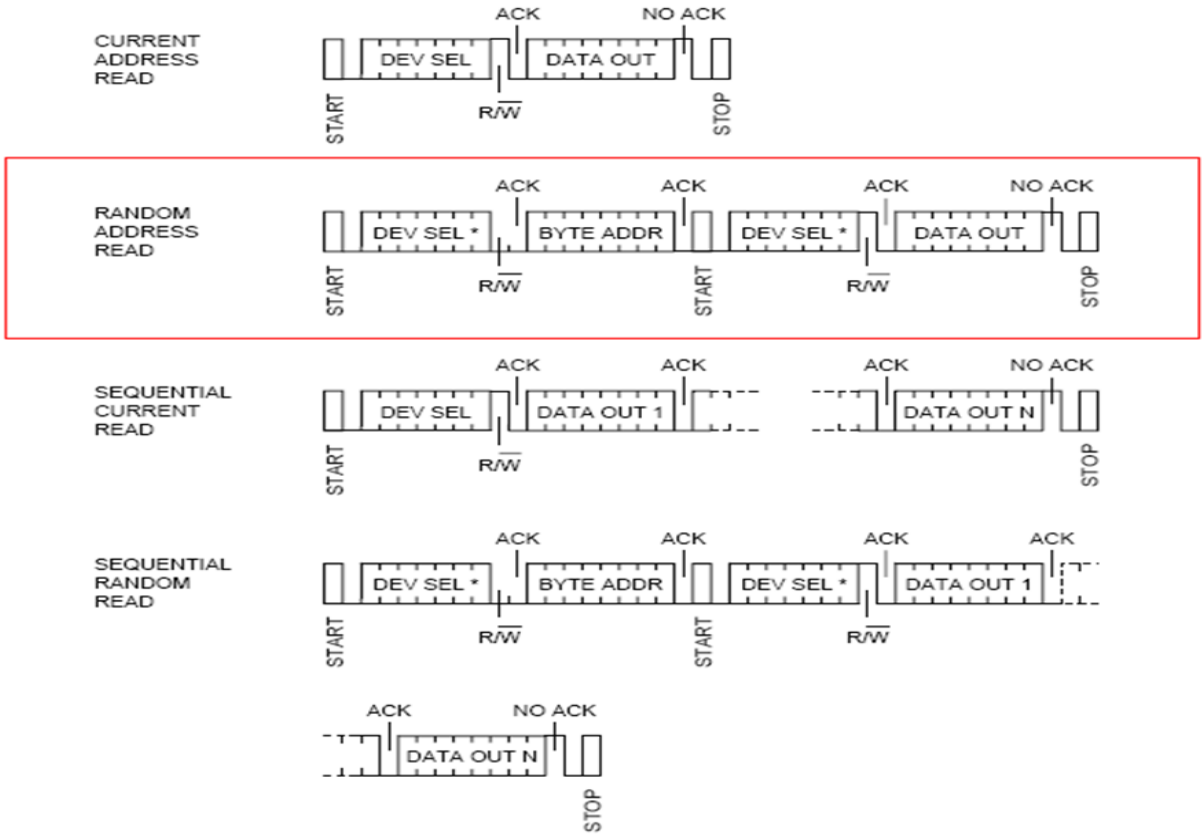


Figure 5-11: I2C Write Sequence (2)

5.2.2 I2C Command

- Slave id: default is 0x7F (2-bit from I/O pin: SID1, SID0)
  - Iocfg: 0x380d default value: 0xFF,
    so first time I2C is set to default function, then master can reset iocfg to disable default function.
  - iocfg[1]: i2c_ref_cs, i2c default is not to reference spi_cs to start i2c.
    set to 1, reference slave id to enable i2c
    spi_cs = 0 is to start so initial master send spi_cs to 0 and mode to 0 to select i2c mode, wait sometime, change spi_cs to 0 to enable i2c r/w.
  - iocfg[0] : i2c_lea_cs, i2c default is not reference spi_cs to leave state.
    set to 1 : use stop to leave state
    spi_cs is from 1'b0 to 1'b1 to leave i2c state machine. if i2c_lea_cs is disable, then i2c only reference stop to leave state.

- In write command:

  byte 1 is slave id + R/W (write is 0, read is 1)

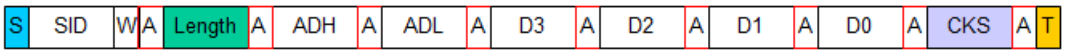
  byte 2 is crc calculation length. When zero, crc is disable;

  when 0xFF, inc_adr_dis is 1 : to disable address increment.

  byte3 is address high : address[15:8]

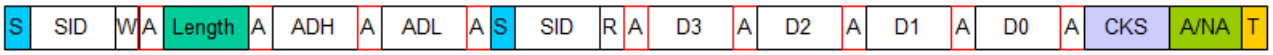
  byte4 is address low : address[7:0]

Write Command

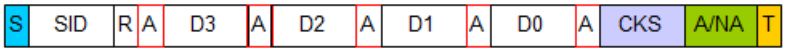


Read Command

Sequential Random address read



Sequential current address read



S : Start ; T : Stop

A : ACK

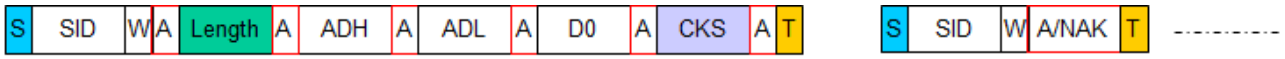
NA : No ACK

Figure 5-12: I2C with CRC

5.2.3 I2C OTP one byte with CRC

Write OTP Command, length = 1 (with crc), 0 (disable crc)

When master write one byte data, and send stop command to start otp write cycle.



If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, the Start bit and control byte must be re-sent. If the cycle is complete, the device will return the ACK and the master can then proceed with the next Read or Write command.

5.3 UART

5.3.1 UART Config

- iocfg : 0x380d default value: 0xFF,
  so first time UART is set to default function, then master can reset iocfg to disable default function.
- iocfg[7]: uart_ref_cs ,uart default is not to reference spi_cs to start uart.
  set to 1, using slave_id to enable uart function
  (spi_cs = 0 is to start. so initial master send spi_cs to 1 and mode to 0 to select uart mode, wait sometime, change spi_cs to 0 to enable uart r/w)
- iocfg[6]: uart_lea_cs, uart default is not to reference spi_cs to leave state.
  set to 1, using timeout to leave state.
  (spi_cs is from 1'b0 to 1'b1 to leave uart state machine. When read, master can use NACK or spi_cs to leave uart state)
- iocfg[5]: uart_bau_en uart defalut is to enable baud rate detection.

5.3.2 UART Slave ID

- slaveid[7:0]: 0x380F
  - slaveid[7]: default is high.
    if this bit is set to high, the general call address (00h) is recognized, otherwise it is ignored.
  - uart_slave_id[5:0] = {slaveid[5:0],slaveio};
  - slave io = {**SID1** pin, **SID0** pin}, 2bit

- iocfg[4:2] : To select time out period
  - 3'd7 : 2^21 * sys_clk (default setting)
  - 3'd6 : 2^20 * sys_clk
  - 3'd5 : 2^19 * sys_clk
  - 3'd4 : 2^18 * sys_clk
  - 3'd3 : 2^17 * sys_clk
  - 3'd2 : 2^16 * sys_clk
  - 3'd1 : 2^15 * sys_clk
  - 3'd0 : 2^14 * sys_clk
  - If default sysclk is 16MHz, then time out is equal to 62.5ns * 2^21 = 131ms.
  - If default sysclk is 4MHz, then time out is equal to 250ns * 2^21 = 524ms.

5.3.3 UART Command

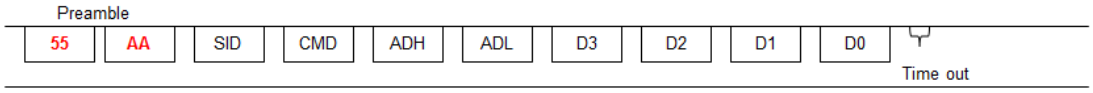
- uart_cmd[7]: inc_adr_dis,
  1: to disable address increment.
  ex: reading dsp_status [DSPRDY, STOP, TRIGCNT] (cfg addr = 16'h387a).
  If DSPRDY is from 0 to 1, then master can read out dsp out buffer data.
- uart_cmd[6:4]: Read/write command
  uart_cmd[6:4] = 3'h1 for read with crc enable
  uart_cmd[6:4] = 3'h2 for write with crc enable
  uart_cmd[6:4] = 3'h3 for read with crc disable
  uart_cmd[6:4] = 3'h4 for write with crc disable
- uart_cmd[3:0]: Read/Write package number
  case1: crc enable, set to 4, master must send out 4byte data + 1byte crc. Then slave will send out 0x5A(ack)/0xA5(nack).
  case2: crc disable, set to 4, master must send out 4byte data. Then slave will not send out 0x5A(ack)/0xA5(nack).
- When length = 0, then hardware (IC) will set the internal length equal to d'96 so FW can read the data of dsp outbuf by 4 times (96*4 = 384 bytes) with crc.
- When crc is disable, the length setting is needed, the state machine is left when time_out.
- uart protocol : start bit + 8bit data + stop bit, no parity bit (10bit)
- 0x55 1byte for baud rate detection
- 0xAA, slave check if baud rate is the same as master.
  - If the same, slave send out 0x5A (Ack), no send out.
  - If not the same, slave send out 0xA5 (NAck), no send out.
- When write command, if slave crc is the same as master crc, then slave send out 0x5A(Ack), not the same, slave send out 0xA5(Nack).
- In write command :
  - If in the time out period, the master sends out another data series, the write state machine will go on writing action. (Address auto increment)
- If time out is got, then the write state machine will go to idle state. Then another write/read command can work.
- otp write time :
  - parameter Tpw_min = 90000 ; //Min Program Pulse Width Time
  - parameter Tpw_max= 110000; //Max Program Pulse Width Time
- In read command:
  - When the read package is end, the master can send out 0x5A for continuing to read

another data package (address auto increment); or 0xA5 for stopping the read action, then the read state machine will go to idle state; or wait time out to idle state.

- If spi_cs is to be referenced, then spi_cs from 0 to 1, then the read state machine will go to idle state.

5.3.4 UART without CRC

Write Command



Read Command

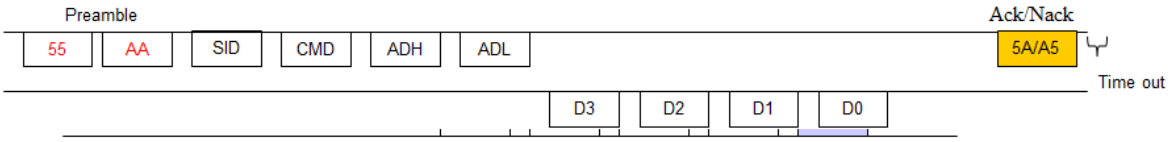
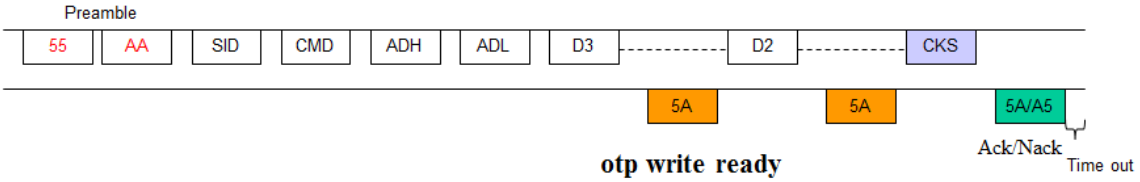


Figure 5-13: UART without CRC

5.3.5 UART OTP one byte with CRC

Write Command



Read Command

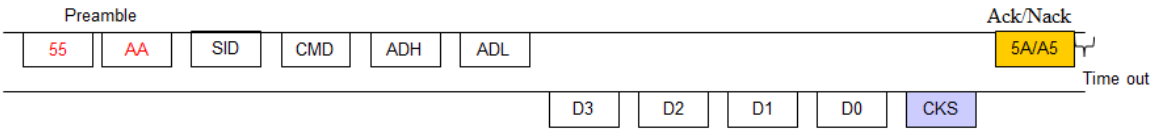


Figure 5-14: UART OTP one byte with CRC

5.4 GPIO

The PL7211 has 9 GPIO pins. These can be configured to be input or output by DSP or register setting.

- locfg[3]: GPIO direction control by DSP or register setting
  1: control by DSP
  0: control by CFG register

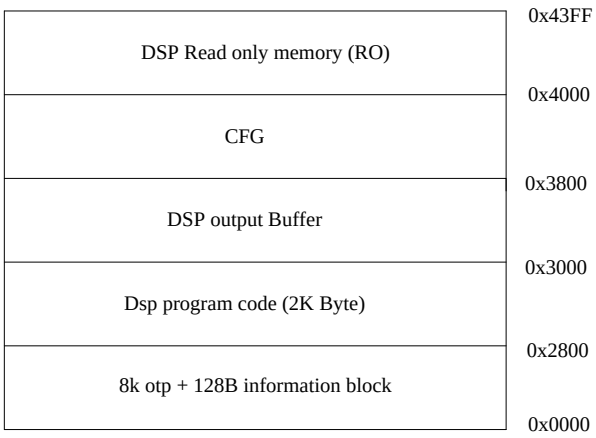
- These can be disabled/enabled:
  reg_pinfunc_P00[1:0]:
  00:GPIO other: special function
- The definitions of reg_pinfunc_P01[1:0] ~ reg_pinfunc_P14[1:0] is the same as reg_pinfunc_P00[1:0].
- The settings can be read out from:
  Address 0x3903: GPIO pins DIR[15:8]
  Address 0x3902: GPIO pins DIR[7:0]
  Address 0x3905: GPIO pins DATA[15:8]
  Address 0x3904: GPIO pins DATA[7:0]
- The GPIO data can be written by DSP firmware, for example:

```
SUBM    R6   xx   GPI_04   R2          // input button GPI_04
STR     GPO_13   R6       0           // Relay output to GPO_13
```

6. Memory Mapping Overview

The PL7211 memory space mapping shown in Figure 6-1 depicts the addressing space and range of each memory macro or register. This memory space is accessible through the SPI/UART/I2C interface of PL7211. The main function of each addressing space is:

- **Configuration (CFG) register**: Various settings, such as DSP options, AVM/MS options and GPIO options, are configured by CFG register. For more details, please see the CFG register section.
- **DSP Buffer**: The calculated energy information located in DSP buffer can be obtained through the SPI/UART/I2C interface of PL7211.
- **DSP Code RAM**: The DSP code RAM stores the program executed by DSP after power on sequence of PL7211 is accomplished.
- **MTP Memory**: MTP (Multi-Time Programmable) memory which is a non-volatile memory stores the DSP code and register configurations. After power-on, the POS (power on sequence) copies the contents of MTP memory to DSP code RAM and CFG registers, respectively. When the POS is done, PL7211 starts to execute based on the DSP code RAM and CFG register settings.



address decode		real address position
0x0000~0x27FF	: 8k OTP + 128B	(0x0000~0x207F)
0x2800~0x2FFF	: 2k dsp prog	(0x2800~0x2FFF)
0x3000~0x37FF	: 2k dsp buf	(0x3000~0x317f)
0x3800~0x3FFF	: 2k cfg	(0x3800~0x39FF)
0x4000~0x43FF	: 1k dsp ro	(0x4000~0x43FF)

Figure 6-1: PL7211 Memory Mapping

6.1 MTP memory mapping

The MTP (Multi-Time Programmable) memory which is a non-volatile memory stores the DSP code and register configurations. As shown in Figure 6-2, the MTP memory space is divided into two main sections, which are space for CFG register and for DSP code, respectively.

Due to the one-time programming property of MTP memory, the DSP program section and CFG data section of MTP memory are partitioned into multiple banks for multi-programming times.

The DSP program section of MTP is divided into 3 banks. The size of each bank is 2K Bytes. The CFG data section of MTP is divided into four banks. The size of each bank is 256 bytes.

Only the newest DSP program bank and the newest CFG data bank will be copied into DSP code RAM and CFG registers respectively. It should be programmed from the lowest bank # of DSP/CFG section.

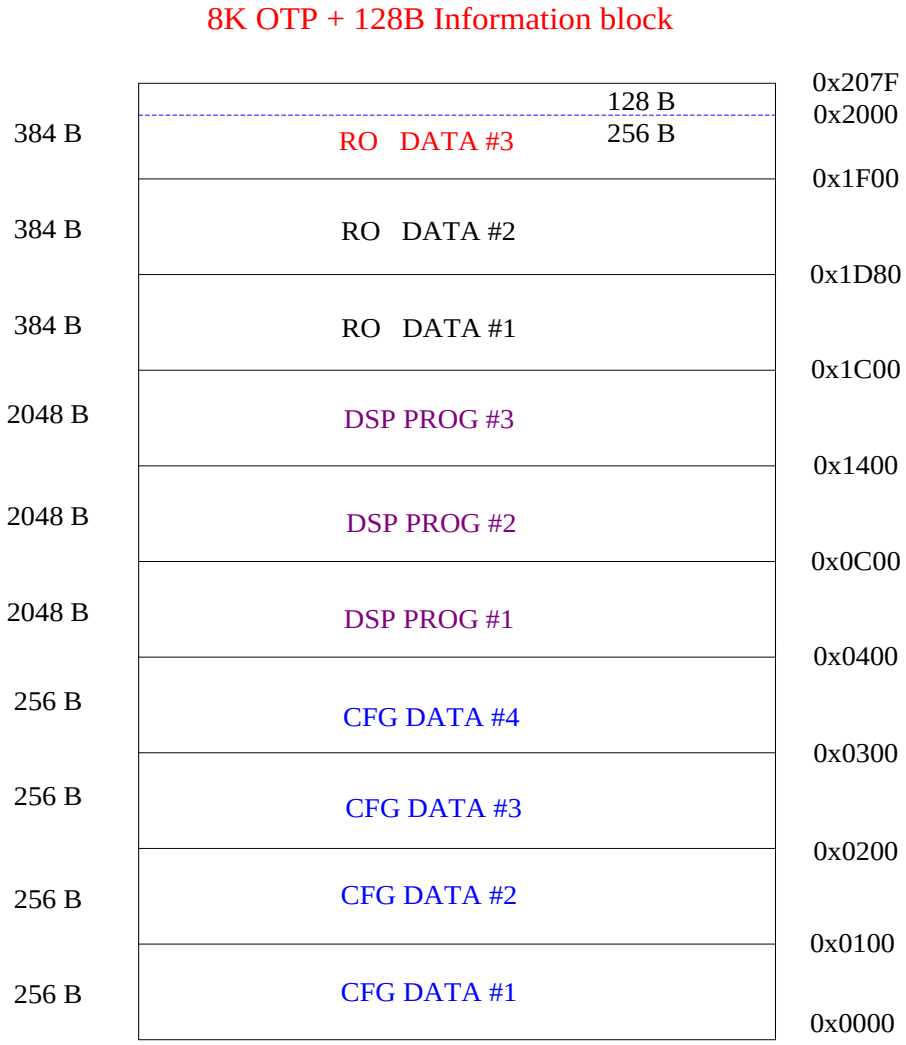


Figure 6-2: MTP Memory Mapping Diagram

7. Power-On Sequence (POS)

When power turns on or external reset is released, the POS copies the MTP memory contents to CFG register and DSP code RAM, respectively. After POS operation, the DSP starts to execute. The POS operating procedure is shown as Figure 7-1.

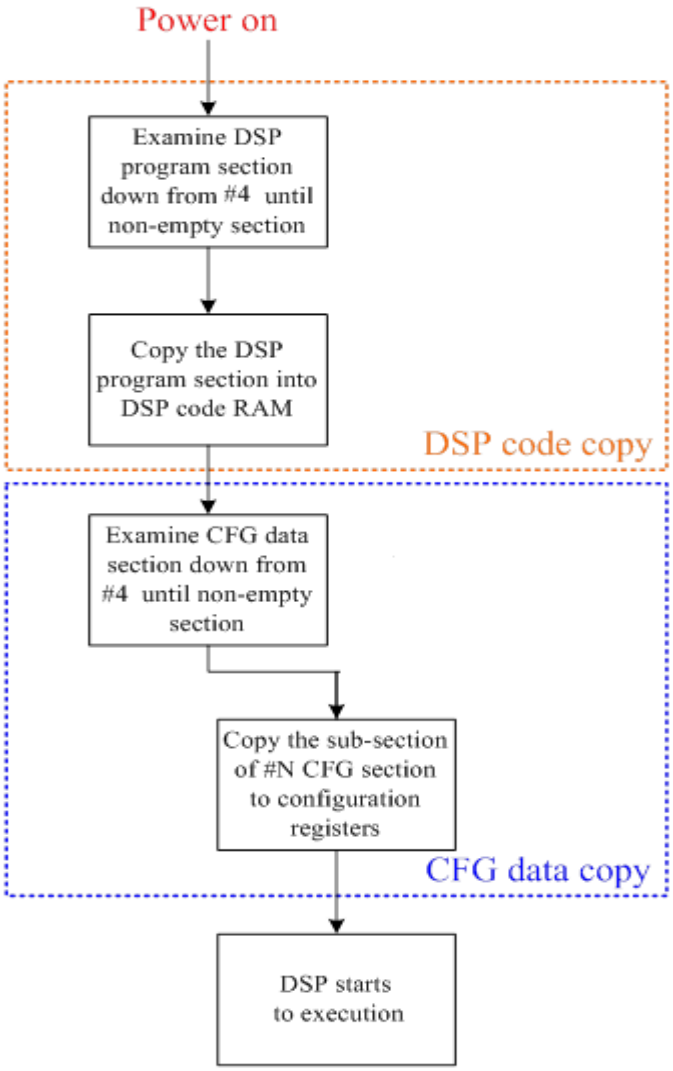


Figure 7-1: POS Sequence

7.1 POS example

Figure 7-2 is a POS example based on the following conditions. In such condition, POS copies CFG DATA #2 from MTP to CFG register, copies DSP bank #3 to DSP code RAM, and copies RO DATA#2 from MTP to RO RAM.

Example Condition:

- CFG DATA 1 and 2 are programmed and bank 3 and 4 are empty.
- DSP PROG 1~3 are programmed.
- RO DATA 1 and 2 are programmed and DATA3 is empty.

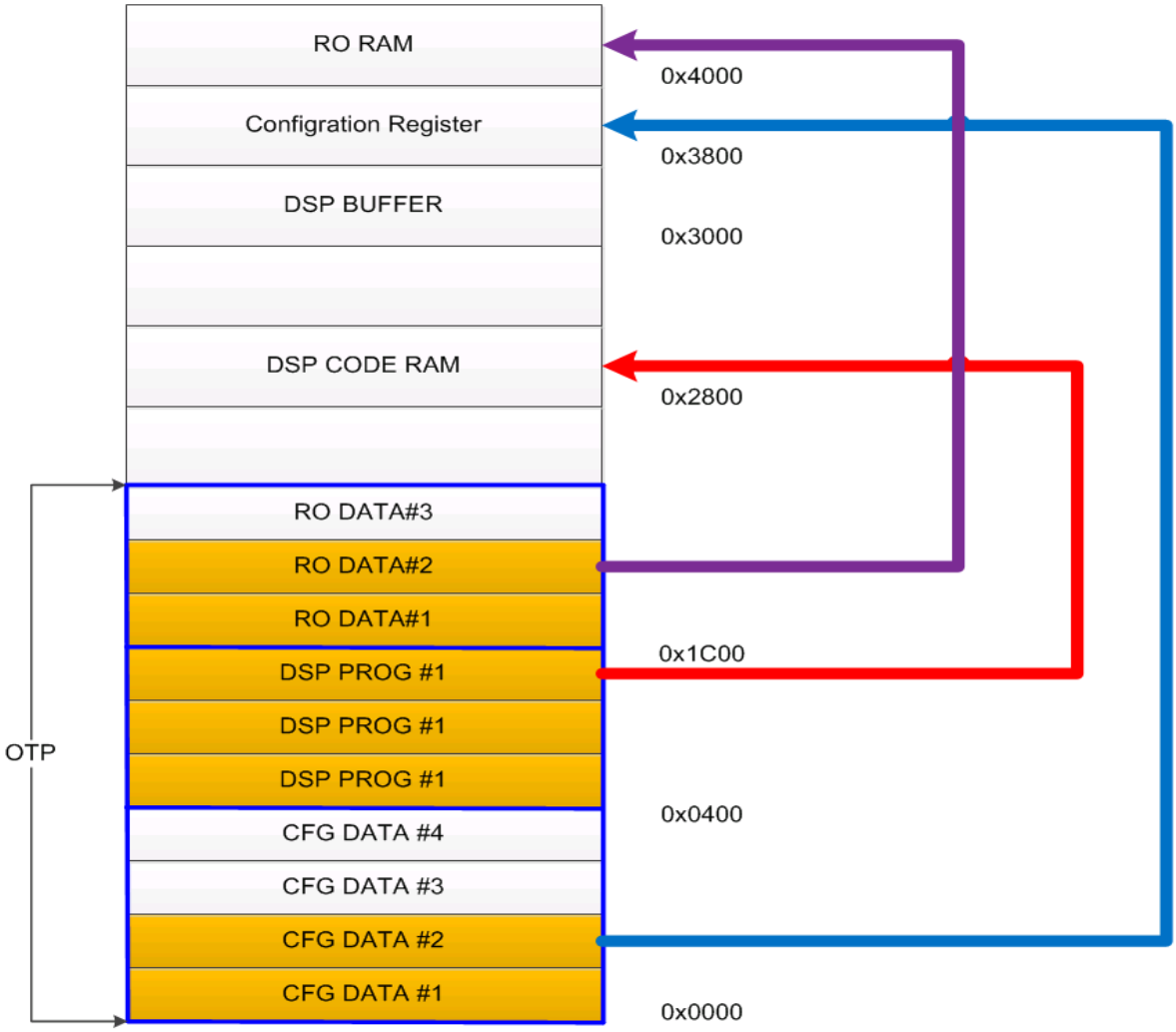
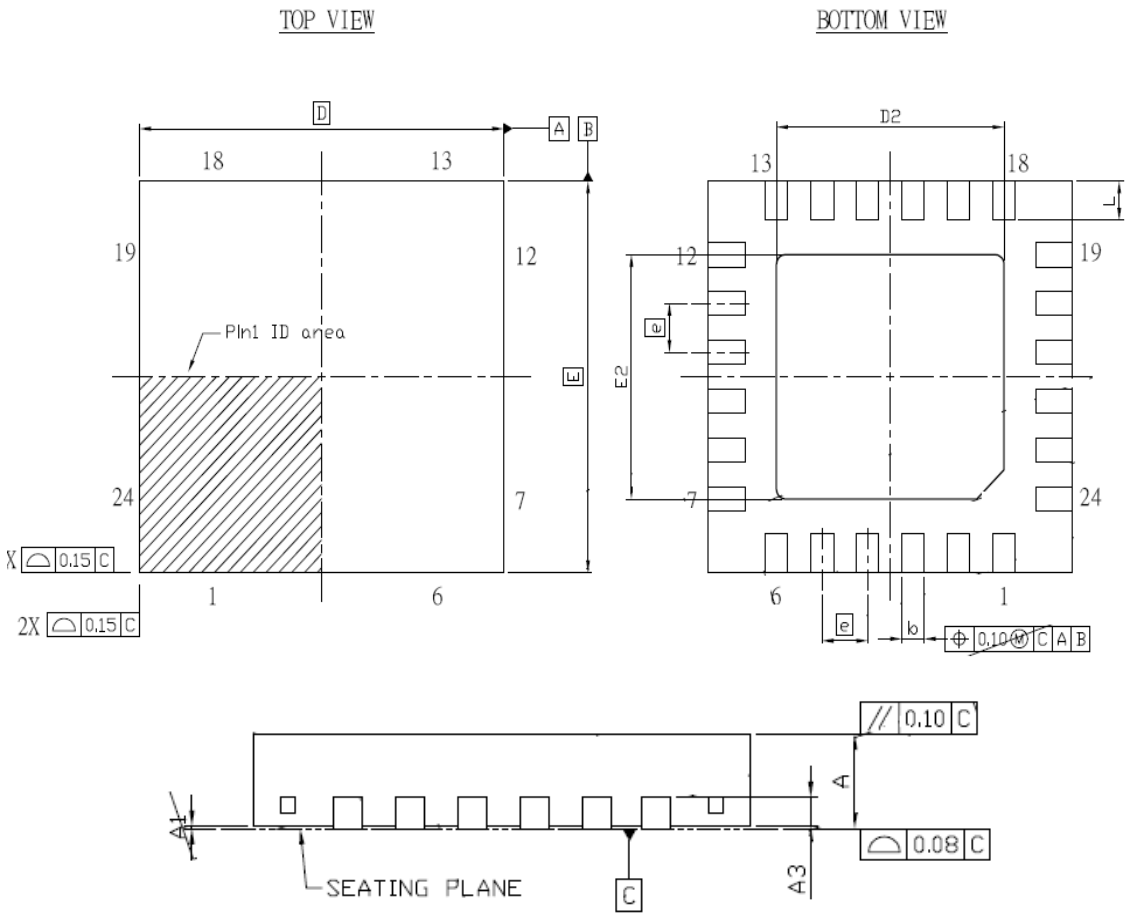


Figure 7-2: POS Sequence Example

8. Package Outline Dimension

8.1 24-Pin QFN Package (4x4)



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.5	29.5	31.5
A1	0	0.02	0.05	0	0.79	1.97
A3	0.203 REF			8 REF		
b	0.18	0.25	0.30	7.1	9.8	11.8
D	3.90	4.00	4.10	153.5	157.5	161.4
D2	2.40	2.50	2.60	94.5	98.4	102.4
E	3.90	4.00	4.10	153.5	157.5	161.4
E2	2.40	2.50	2.60	94.5	98.4	102.4
e	0.50 BSC			19.7 BSC		
L	0.30	0.40	0.50	11.8	15.7	19.7

Figure 9-1: PL7211 Package Outline Diagram (QFN24 4x4)

9. ORDERING INFORMATION

Table 10-1：Ordering Information

Model/Device	Package Type	Pins	Package Qty	Prolific Type Code	ECO
PL7211	QFN	24	4000pcs / Reel	PL7211C1FIG8P1	Green (RoHS)
PL7211	QFN	24	4900pcs / Tray	PL7211C1FIG7P1	Green (RoHS)

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