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# Application Note
# PL-2571 (Chip Rev B) Hi-Speed USB to SATA Bridge Controller PCB Layout Guide

## Introduction

This document explains how to design a PCB for PL-2571B Hi-Speed USB-to-SATA Controller device with the following goals in mind:

1. Make a noise-free, power-stable environment suitable for the PL-2571B.

2. Reduce the possibility of EMI and EMC.

3. Simplify the task of routing signal trace to make a better design circuit.

## Placement

The following are the guidelines for an ideal placement:
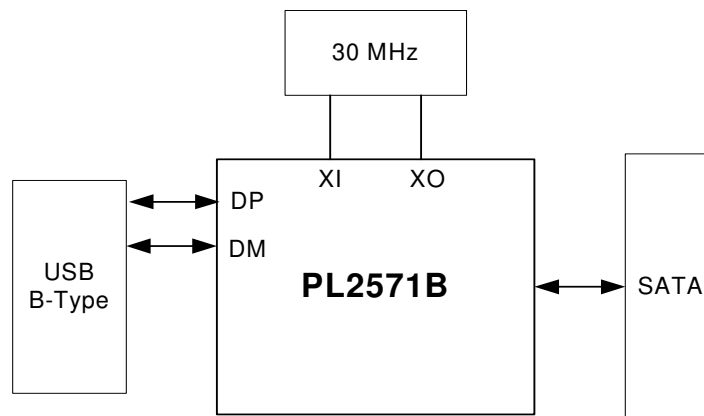


- Always primarily consider in placement the TXDP/RXDP/TXDN/RXDN four SATA traces.

- The distance between USB_B-type to PL-2571B should be as short as possible. Connect DP and DM from the USB B-Type connector to DP (Pin-41) and DM (Pin-42) directly.

- The distance between the Crystal to PL-2571B XI and XO should also be as short as possible.

- Crystal should not be placed near I/O ports, board edges, and other high-frequency devices or traces (such as Power signal) or magnetic field devices (such as magnetic).

- The outer shield of Crystal needs well grounding to prevent EMC/EMI from inducing extra noise. The retaining straps of the Crystal also need well grounding.

- High Current devices should be placed near the Power source to reduce the trace length. Traces with high current will induce more EMI.

- Route USB 2.0 differential pairs near non-USB 2.0 I/O connectors, signal headers, crystals, oscillators, magnetic devices, and power connectors.

## Trace Routing

Good routing of traces can reduce the propagation delay, cross talk, and high-frequency noise. It can also improve the signal quality for the receiver and reduce the loss from transmitted signals.

- Avoid routing to break image plane (anti-etch areas) – Route SATA differential signal pair traces over continuous ground and power planes. Avoid crossing anti-etch areas or any break in the underlying planes. Don't route SATA differential signal pair trace under crystal, oscillator, clock synthesizers, magnetic devices or IC as this would cause interference.



Plane 1          Plane 2
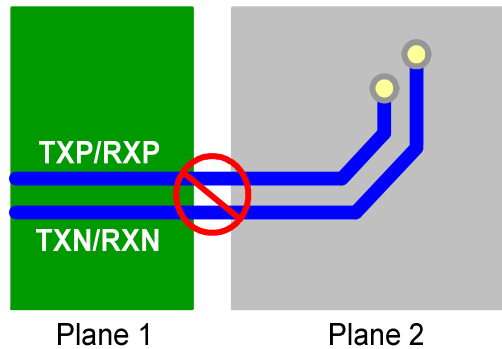
- Avoid signal reflection – Route SATA differential signal pair should not change layer by vias [see below Figure no. 3], and avoid branch trace by via [see below Figure no. 2]. These can reduce signal reflection and impedance change. If it is necessary to turn 90° [see Figure below no. 1], it is better to use two 45° turn or an arc instead of making a single 90° turn. This can reduce reflection on the signal by minimizing impedance discontinuities.



Ground Plane
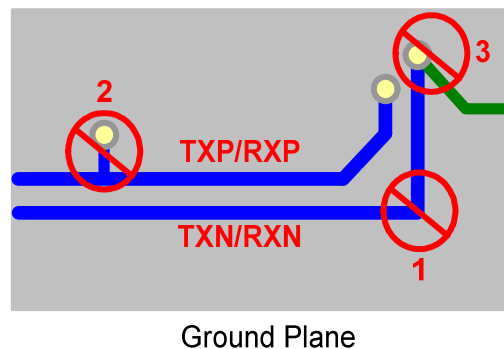
- Avoid stubs on differential pair trace – Stubs on USB 2.0 differential signal pair should be avoided. While stubs exist, it will cause signal reflection and affect signal quality. If a stub is unavoidable in the design, shorten the stub length as much as possible.



Ground Plane
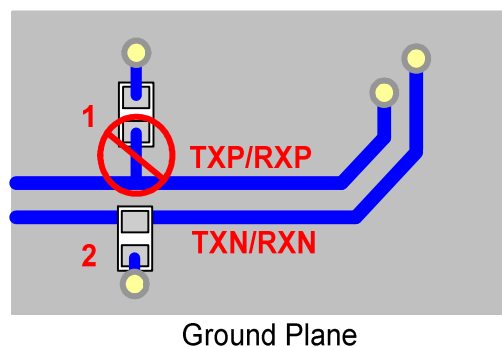
- The capacitors located within the TXDP/RXDP and TXDN/RXDN path should be close to the SATA connector as much as possible.
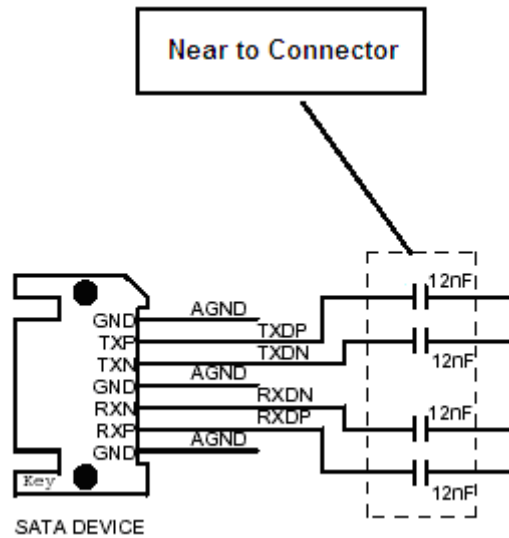


- The four trace lengths of TXDP/RXDP/TXDN/RXDN should be equal or less than 630 mil if possible.

- Spaces between TX and RX should be larger than 35 mil.

- Recommend test board should consist of differential traces (100 ohm ± 15 ohm) over a ground plane (single ended 50 ohm ± 5 ohm). Refer to below suggested Trace Width and Trace Separation for different double-sided PCB thickness. Consult your PCB vendor for more information.

| Double-sided PCB Thickness | W2 (Trace Width) | S1 (Trace Separation) | Differential Impedance |
|---|---|---|---|
| 1.0mm | 14.5 mil | 7.0 mil | 100.72 |
| 1.2mm | 15.0 mil | 7.0 mil | 100.66 |
| 1.6mm | 16.0 mil | 7.0 mil | 100.04 |

**Double-Sided PCB Thickness: 1.0mm**

**Double-Sided PCB Thickness: 1.2mm**
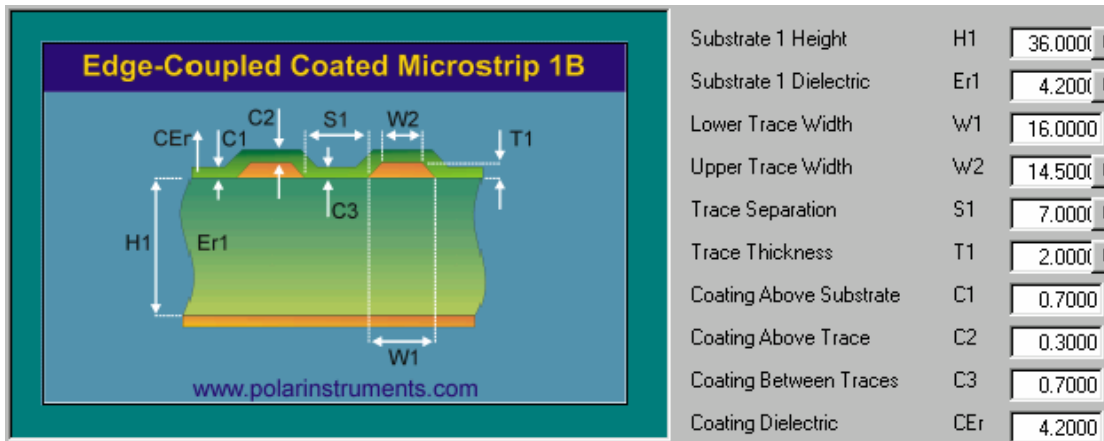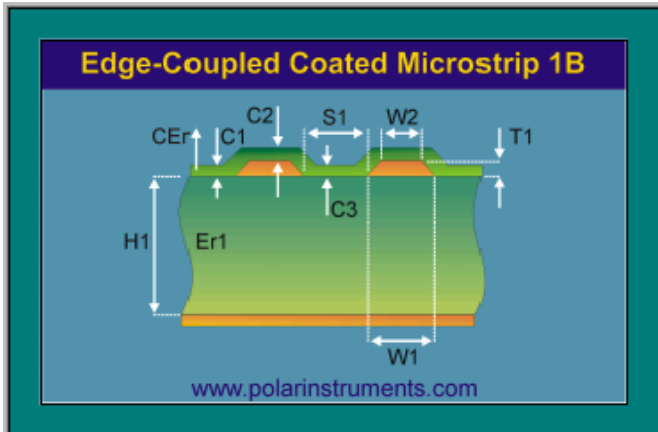


| Edge-Coupled Coated Microstrip 1B | | |
| --- | --- | --- |
| Substrate 1 Height | H1 | 43.0000 |
| Substrate 1 Dielectric | Er1 | 4.2000 |
| Lower Trace Width | W1 | 17.0000 |
| Upper Trace Width | W2 | 15.0000 |
| Trace Separation | S1 | 7.0000 |
| Trace Thickness | T1 | 2.0000 |
| Coating Above Substrate | C1 | 0.7000 |
| Coating Above Trace | C2 | 0.3000 |
| Coating Between Traces | C3 | 0.7000 |
| Coating Dielectric | CEr | 4.2000 |

**Double-Sided PCB Thickness: 1.6mm**
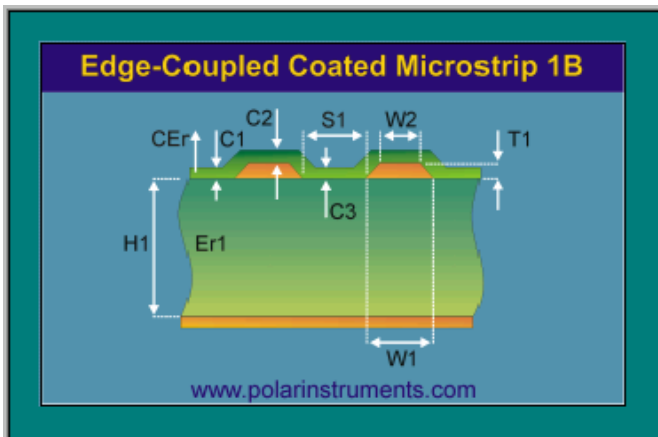


| Edge-Coupled Coated Microstrip 1B | | |
| --- | --- | --- |
| Substrate 1 Height | H1 | 55.0000 |
| Substrate 1 Dielectric | Er1 | 4.2000 |
| Lower Trace Width | W1 | 18.0000 |
| Upper Trace Width | W2 | 16.0000 |
| Trace Separation | S1 | 7.0000 |
| Trace Thickness | T1 | 2.0000 |
| Coating Above Substrate | C1 | 0.7000 |
| Coating Above Trace | C2 | 0.3000 |
| Coating Between Traces | C3 | 0.7000 |
| Coating Dielectric | CEr | 4.2000 |

- Avoid right angle signal traces:
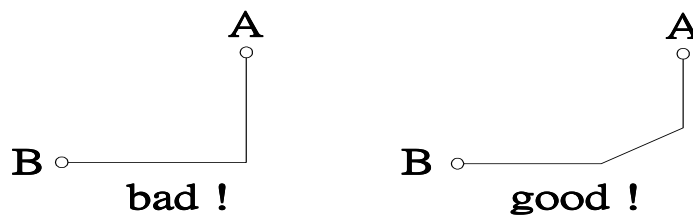


- Avoid digital signals that interfere with analog signals (crystal clock) and Power trace.

- The trace length and the ratio of trace width to trace height above the ground planes should be considered carefully. The clocks and other high speed signal traces should be as short and wide as possible (compare with normal digital trace). It is better to have a ground plane under these traces, and if possible, with GND plane around.

- The trace of Power signal should be short and wide.

- The trace length between crystal and XI, and the trace length between crystal and XO should be equal.

- The traces listed below should be wider and short as possible. The traces should also not cross any signal traces.

  ➢ The traces between the crystal and XI, XO.

  ➢ The traces between USB connector and DM, DP, DMRS, DPRS.

  ➢ The traces between the capacitors and the regulator input, output, and ground.

- The trace length between USB connector and DM, and the trace length between USB connector and DP should be equal.

## Design of Via

- The distances between the vias should be kept as apart as much as possible.

- The traces of differential pairs should have at least two vias and should avoid more than two.

- Two traces in differential pair should have identical number of vias and should have identical bounding pad shape and size.

- Through-hole via should be avoided as much as possible. There should be enough space between the through-hole and the adjacent metal on the PCB.

## Power and Ground Planes

- 3.3V power: support PL-2571B and other devices. Avoid using unnecessary power trace to PL-2571B and keep these traces short and wide.

- GND plane - You can separate the digital GND to Analog GND as follows: Partition of GND plane needs experience and experiment. The key point is to keep the return path of analog GND almost the same to the common GND. If you do not feel confident on this, simply leave the GND plane unchanged (i.e. no partition at all).

- For all partition on Power/GND plane, right angle is not recommended. This is the same to the signal/power/bus traces.

## For Better and More Stable Analog Performance

- When using 30MHz crystal as clock source, you should pay more attention to the specification of crystal. Please refer to the USB crystal spec. When using crystal as specification, two matching caps (10pF in schematic) should be attached to the XI and XO pin.

- When using oscillator as clock source (30MHz), avoid attaching any cap on the clock trace.

- GND plane partition is not recommended, please keep the GND plane as large and clear as possible.

## Intel Layout Recommendations for SATA and USB 2.0 Guidelines

Following are taken from Intel Chipset Platform Design Guide for SATA and USB 2.0 Interface Layout Recommendations:

- With minimum trace lengths, route high-speed clock and USB differential pairs first.

- Route SATA/USB signals ground referenced.

- Route SATA /USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes. Use a maximum of 2 vias per trace. Vias should be matched on traces within a transmit or receive pair.

- When it becomes necessary to turn 90 degrees, use two 45-degrees turns or an arc instead of making a single 90 degree turn. This reduces reflections on the signal by minimizing impedance discontinuities.

- Do not route SATA/USB traces under crystals, oscillators, clock synthesizers, magnetic devices, or ICs that use and/or duplicate clocks.

- Stubs on USB signals should be avoided as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the sum of all stubs on a given data line should not be greater than 200 mils.

- Route all traces over continuous planes (GND) with no interruptions. Avoid crossing over anti-etch if possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces.

- Keep traces at least 90 mils away from the edge of the plane (VCC or GND depending on which plane to which the trace is routed). This helps prevent the coupling of the signal onto adjacent wires and helps prevent free radiation of the signal from the edge of the PCB.

- Maintain parallelism between SATA differential signals with the trace spacing needed to achieve $100\Omega \pm 15\%$ differential impedance.

- Maintain parallelism between USB differential signals with the trace spacing needed to achieve $90\Omega$ differential impedance.

- Minimize the length of high-speed clock and periodic signal traces that run parallel to SATA/USB signal lines to minimize crosstalk. The minimum recommended spacing to clock signals is 50 mils.

- Use 20-mil minimum spacing between SATA/USB signal pairs and other signal traces. This helps to prevent crosstalk.

- SATA/USB signal pair traces should be trace length matched. Max trace length mismatch between SATA signal pair (such as TXN and TXP) or USB signal pair (such as DM1 and DP1) should be no greater than 150 mils.

- In certain systems where a short, very low loss cable is to be exclusively used, it may be desirable to use longer trace lengths to optimize SATA signal quality at the device receiver (RX connector specification). Careful simulation and/or studies on prototypes of signal quality are required to balance this trade off effectively.