Application Note
PL-2303 USB to Serial Bridge Controller PCB Layout Guide

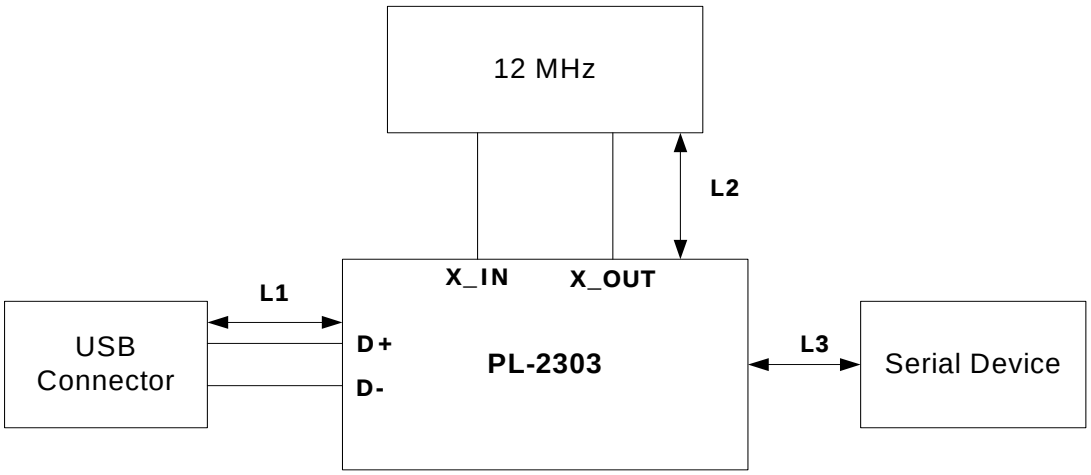
Introduction

This document explains how to design a PCB for Prolific PL-2303 USB-to-Serial Bridge Controller with the following goals in mind:

1. Make a noise-free, power-stable environment suitable for the PL-2303.
2. Reduce the possibility of EMI and EMC.
3. Simplify the task of routing signal trace to make a better design circuit.

Placement

The following are the guidelines for an ideal placement:

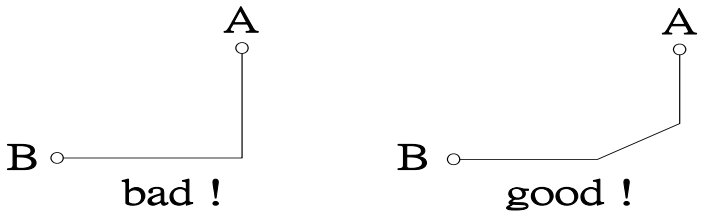


- The distance between USB connector to PL-2303 (L1) should be as short as possible. Connect DP and DM from the USB B-Type connector to DP (Pin-56) and DM (Pin-55) directly.
- The distance between the Crystal to PL-2303 OSC1 and OSC2 (L2) should also be as short as possible.
- Crystal should not be placed near I/O ports, board edges, and other high-frequency devices or traces (such as Power signal) or magnetic field devices (such as magnetic).
- The outer shield of Crystal needs well grounding to prevent EMC/EMI from inducing extra noise. The retaining straps of the Crystal also need well grounding.
- High Current devices should be placed near the Power source to reduce the trace length. Traces with high current will induce more EMI.
- The traces between PL-2303 and serial device also must be short as possible. This is important but for practical implementation convenience, this could be sacrificed

Trace Routing

Good routing of traces can reduce the propagation delay, cross talk, and high-frequency noise. It can also improve the signal quality for the receiver and reduce the loss from transmitted signals.

- Avoid right angle signal traces:



- Avoid digital signals (such as RS232 signals) that interfere with analog signals (crystal clock) and Power trace.
- The trace length and the ratio of trace width to trace height above the ground planes should be considered carefully. The clocks and other high speed signal traces should be as short and wide as possible (compare with normal digital trace). It is better to have a ground plane under these traces, and if possible, with GND plane around.
- The trace of Power signal should be short and wide.
- Connect a 10uF and 0.1uF capacitor between REG_IN (VDD_5 Pin20) and REG_GND, and connect a 10uF and 0.1uF capacitor between REG_VO (pin17) and GND.
- The trace length between crystal and XIN, and the trace length between crystal and XOUT should be equal.
- The traces listed below should be wider and short as possible. The traces should also not cross any signal traces.
    - The traces between the crystal and XIN, XOUT.
    - The traces between USB connector and X_DN, X_DP.
    - The traces between the capacitors and REG_VIN.
    - The traces between the capacitors and REG_VO.
    - The traces between the capacitors and REG_GND.
- The trace length between USB connector and X_DN, and the trace length between USB connector and X_DP should be equal.

Power and Ground Planes

- GND plane - Separate the digital GND to Analog GND as follows: Partition of GND plane needs experience and experiment. The key point is to keep the return path of analog GND almost the same to the common GND. If you do not feel confident on this, simply leave the GND plane unchanged (i.e. no partition at all).

- For all partition on Power/GND plane, right angle is not recommended. This is the same to the signal/power/bus traces.

For Better and More Stable Analog Performance

- When using 12MHz crystal as clock source, you should pay more attention to the specification of crystal. Please refer to the USB crystal spec. When using crystal as specification, two matching caps (10pF in schematic) should be attached to the XIN and XOUT pin.

- When using oscillator as clock source (12MHz), avoid attaching any cap on the clock trace.

- GND plane partition is not recommended, please keep the GND plane as large and clear as possible.

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