



PL2303SA (SOP8 Package) USB to Serial Bridge Controller Product Datasheet

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Revision History

Revision	Description	Date
1.2.0	➤ Remove Distributors Contact Information (refer to Prolific website instead)	March 27, 2018
1.1.1	➤ Modify Ordering Information	May 4, 2012
1.1.0	➤ Added Reference Schematic ➤ Remove USB Descriptors Information ➤ Added Chip Marking Information	March 30, 2012
1.0.0	➤ Formal Release – PL2303SA Product Datasheet	October 3, 2011

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1.0 Features

- Fully Compliant with USB Specification v2.0 (Full-Speed)
- UHCI/OHCI (USB1.1), EHCI (USB 2.0), xHCI (USB 3.0) Host Controller Compatible
- On Chip USB 1.1 transceiver, 5V→3.3V regulator
- On-chip 96MHz clock generator
- Full-duplex transmitter and receiver (TXD and RXD)
 - 5, 6, 7, or 8 data bits
 - Odd, Even, Mark, Space, or None parity mode
 - 1, 1.5, or 2 stop bits
 - Parity error, frame error, and serial break detection
 - Programmable baud rate from 75 bps to 115 kbps
 - Independent power source for serial interface
 - Works with existing PC COM Port software applications (TXD and RXD)
- Configurable 512-byte bi-directional data buffer
 - 256-byte outbound buffer and 256-byte inbound buffer; or
 - 128-byte outbound buffer and 384-byte inbound buffer
- Provides royalty-free Virtual COM Port (VCP) driver support for:
 - Windows 2000, XP, Vista, and 7 (Microsoft Certified WHQL Logo Drivers)
 - Windows Server 2003, 2008, 2008 R2
 - Windows 8
 - Windows CE 4.2, 5.0, 6.0, and Windows Embedded Compact 7
 - Windows XP Embedded (XPe), Point-of-Service (WEPOS), and POSReady
 - Mac OS 8/9, OS X
 - Linux/Android kernel 2.4.31 and above includes built-in PL2303 drivers
- Small footprint 8-pin SOP IC package

2.0 Functional Block Diagram

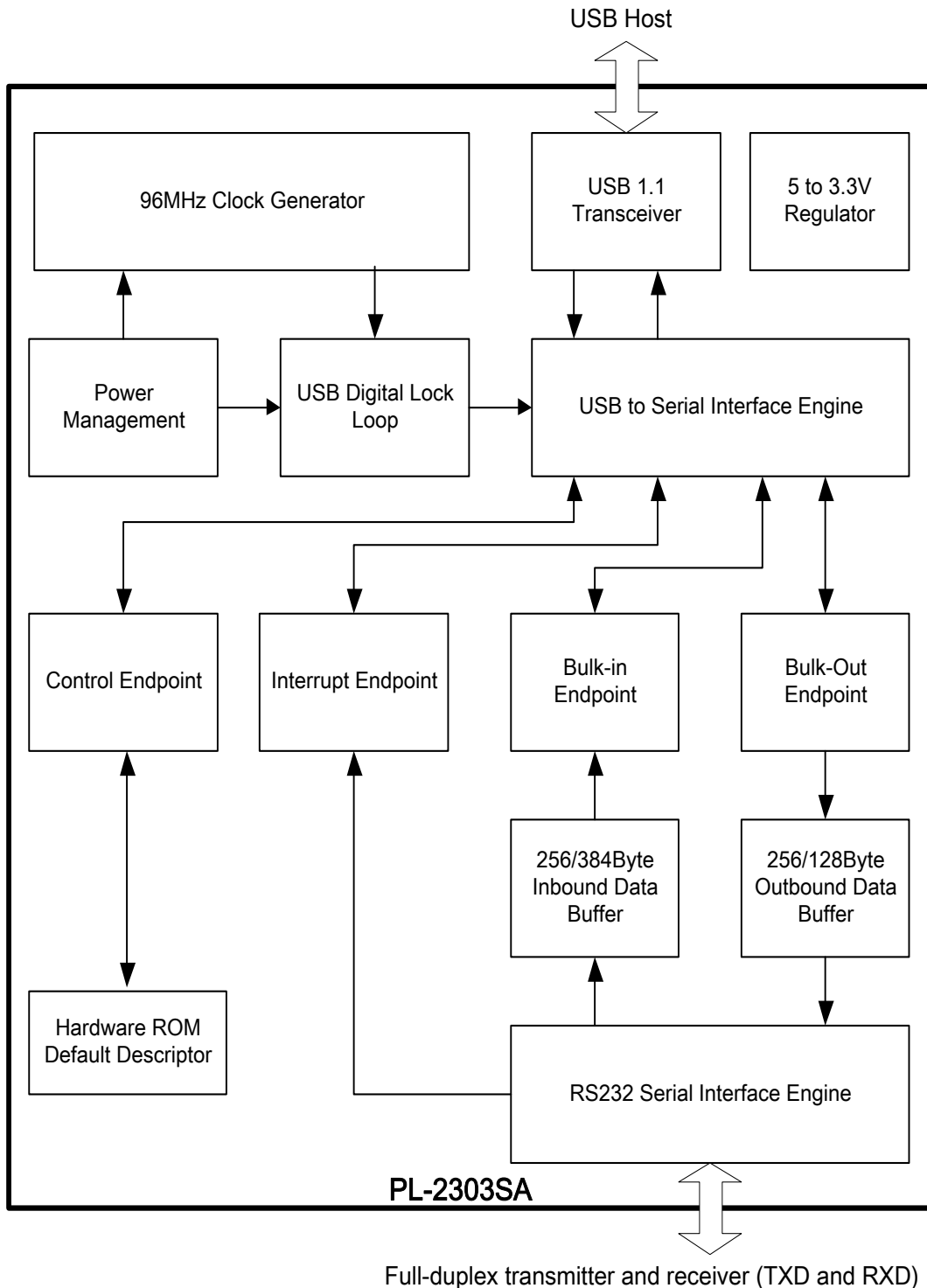


Figure 2-1 Block Diagram of PL2303SA

3.0 Introduction

PL2303SA is a convenient small-factor solution for connecting an RS232-like full-duplex asynchronous serial device (TX-RX only) to any Universal Serial Bus (USB) capable host. Prolific provides highly compatible drivers that could simulate the traditional COM port on most operating systems allowing the existing applications based on COM port (using TX-RX only) to easily migrate and be made USB ready.

By taking advantage of USB bulk transfer mode and large data buffers, PL2303SA is capable of achieving higher throughput compared to traditional UART (Universal Asynchronous Receiver Transmitter) ports. The flexible baud rate generator of PL2303SA also could be programmed to generate any rate between 75 bps to 115 kbps by driver customization.

PL2303SA is exclusively designed for mobile and embedded solutions in mind, providing a very small footprint that could easily fit in to any connectors and handheld devices. With very small power consumption in either operating or suspend mode, PL2303SA is perfect for bus powered operation with plenty of power left for the attached devices. Flexible signal level requirement on the RS232-like serial port side also allows PL2303SA to connect directly to any 3.3V~1.8V range devices.

4.0 Pin Assignment Diagram

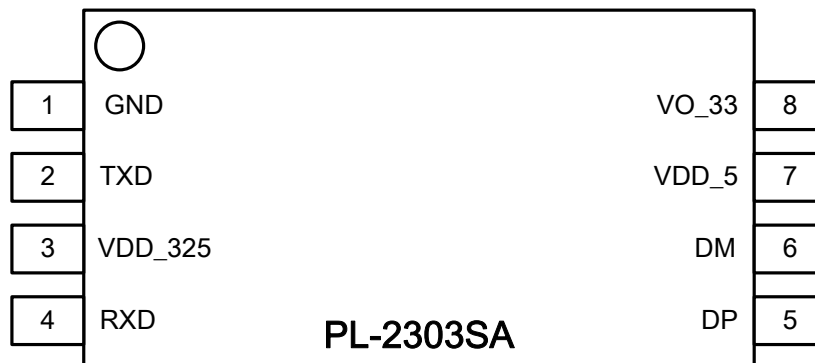


Figure 4-1 Pin Assignment Diagram of PL2303SA SOP8 Package

5.0 Pin Assignment Description

Pin Type Abbreviation:

I: Input	O: Output	B: Bidirectional I/O	P: Power/Ground
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Table 5-1 Pin Assignment Description (SOP8 Package)

Pin #	Name	Type	Description
1	GND	P	Ground
2	TXD	O ⁽¹⁾	Serial Port (Transmitted Data)
3	VDD_325	P	RS232 VDD. The power pin for the serial port signals. When the serial port is 3.3V, this should be 3.3V. When the serial port is 2.5V, this should be 2.5V. The range can be from 1.8V~3.3V.
4	RXD	I ⁽²⁾	Serial Port (Received Data)
5	DP	B	USB Port D+ signal
6	DM	B	USB Port D- signal
7	VDD_5	P	USB Port V _{BUS} , 5V Power
8	VO_33	P	Regulator Power Output, 3.3V

Notes:

(1) – Tri-State, Output Pad. Level and Driving Capability decided by VDD_325.

(2) – Tri-State, CMOS Input/Output Pad with level shifter. Level and Driving Capability decided by VDD_325.

6.0 Data Formats & Programmable Baud Rate Generator

The PL2303SA controller supports versatile data formats and has a programmable baud rate generator. The supported data formats are shown on Table 6-1. The programmable baud rate generator supports baud rates from 75 bps up to 115 kbps as shown in Table 6-2.

Table 6-1 Supported Data Formats

	Description
Stop bits	1 1.5 2
Parity type	None Odd Even Mark Space
Data bits	5, 6, 7, 8

Table 6-2 Driver Supported Baud Rates

Baud Rates (bps)	Baud Rates (bps)	Baud Rates (bps)	Baud Rates (bps)
75	1200	7200	38400
110	1800	9600	56000
150	2400	14400	57600
300	3600	19200	115200
600	4800	28800	

NOTE: Additional baud rate support within the chip specification range can be added by driver customization request. Contact Prolific for more information.

7.0 Application Reference Circuit Diagram

Following is an example of using the PL2303SA as a simple USB to TXD/RXD serial converter. Note that Pin 3 (RS232 VDD) is the power pin for the serial port signals. If Pin 3 is 3.3V, the serial port is 3.3V. If Pin 3 is 2.5V, the serial port is 2.5V. The range can be from 1.8V~3.3V. Contact Prolific FAE for more PCB design support.

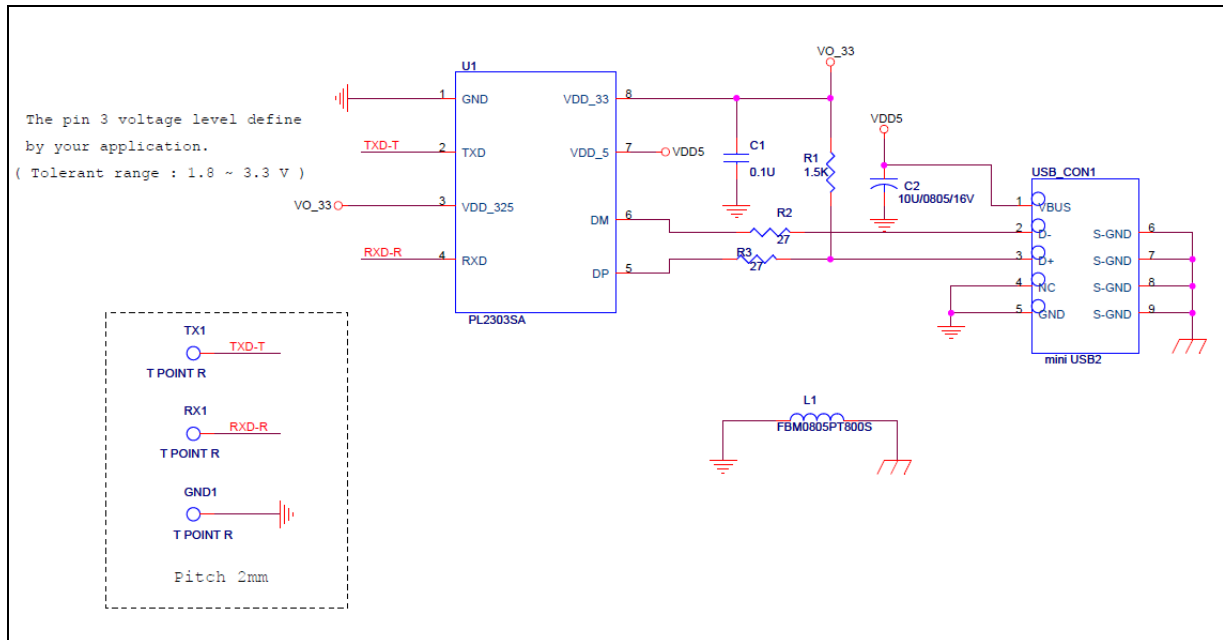


Figure 7-1 PL2303SA Reference Schematic Diagram

8.0 DC & Temperature Characteristics

8.1 Absolute Maximum Ratings

Table 8-1 Absolute Maximum Ratings

Items	Ratings
Power Supply Voltage - VDD_5	-0.3 to 6.5 V
Input Voltage of 3.3V I/O	-0.3 to VO_33+0.3 V
Input Voltage of 3.3V I/O with 5V Tolerance I/O	-0.3 to VDD_5+0.3V
Output Voltage of 3.3V I/O	-0.3 to VDD_5 +0.3 V
Storage Temperature	-40 to 150 °C

8.2 DC Characteristics

8.2.1 Operating Voltage and Suspend Current

Table 8-2a Operating Voltage and Suspend Current

Parameter	Symbol	Min	Typ	Max	Unit
Operating Voltage Range	VDD_5	4.5	5	6.5	V
Output Voltage of Regulator	VO_33	2.97	3.3	3.63	V
Operating Current ⁽¹⁾ (Power Consumption)	I _{DD}	-	20	25	mA
Suspend Current	I _{SUS}	-	260	450	μA

(1) – No device connected.

8.2.2 3.3V I/O Pins

Table 8-2b 3.3V I/O Pins

Parameter	Symbol	Min	Typ	Max	Unit
Output Driving Capability	I _{DD}		4		mA
Power Supply for 3.3V I/O Pins	VO_33	2.97	3.3	3.63	V
Input Voltage (CMOS)					
Low	V _{IL}	--	--	0.3* VO_33	V
High	V _{IH}	0.7* VO_33	--	--	V
Input Voltage (LVTTTL)					
Low	V _{IL}	--	--	0.8	V
High	V _{IH}	2.0	--	--	V
Output Voltage, 3.3V					
Low	V _{OL}	--	--	0.4	V
High	V _{OH}	2.4	--	--	V

8.2.3 Serial I/O Pins

Table 8-2c VDD_325@3.3V Serial I/O Pins

Parameter	Symbol	Min	Typ	Max	Unit
Output Driving Capability	I _{DD}		8		mA
Power Supply for Serial I/O Pins	VDD_325	2.97	3.3	3.63	V
Input Voltage					
Low	V _{IL}	--	--	0.25* VDD_325	V
High	V _{IH}	0.7* VDD_325	--	--	V
Output Voltage					
Low	V _{OL}	--	--	0.4	V
High	V _{OH}	2.4	--	--	V

Table 8-2d VDD_325@2.5V Serial I/O Pins

Parameter	Symbol	Min	Typ	Max	Unit
Output Driving Capability	I _{DD}		5.2		mA
Power Supply for Serial I/O Pins	VDD_325	2.25	2.5	2.75	V
Input Voltage					
Low	V _{IL}	--	--	0.25* VDD_325	V
High	V _{IH}	0.7* VDD_325	--	--	V
Output Voltage					
Low	V _{OL}	--	--	0.4	V
High	V _{OH}	1.85	--	--	V

Table 8-2e VDD_325@1.8V Serial I/O Pins

Parameter	Symbol	Min	Typ	Max	Unit
Output Driving Capability	I _{DD}		4.4		mA
Power Supply for Serial I/O Pins	VDD_325	1.65	1.8	1.95	V
Input Voltage					
Low	V _{IL}	--	--	0.25* VDD_325	V
High	V _{IH}	0.7* VDD_325	--	--	V
Output Voltage					
Low	V _{OL}	--	--	0.4	V
High	V _{OH}	1.25	--	--	V

8.3 Temperature Characteristics

Table 8-3 Temperature Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature	--	0	--	70	°C
Junction Operation Temperature	T _J	-40	25	80	°C

8.4 Leakage Current and Capacitance

Table 8-4 Leakage Current and Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current ⁽¹⁾	I_L	-10	± 1	10	μA
Tri-state Leakage Current	I_{oz}	-10	± 1	10	μA
Input Capacitance	C_{IN}	--	2.8	--	pF
Output Capacitance	C_{OUT}	2.7	--	4.9	pF
Bi-directional Buffer Capacitance	C_{BID}	2.7	--	4.9	pF

(1) – No pull-up or pull-down resistor.

9.0 SOP8 Outline Diagram

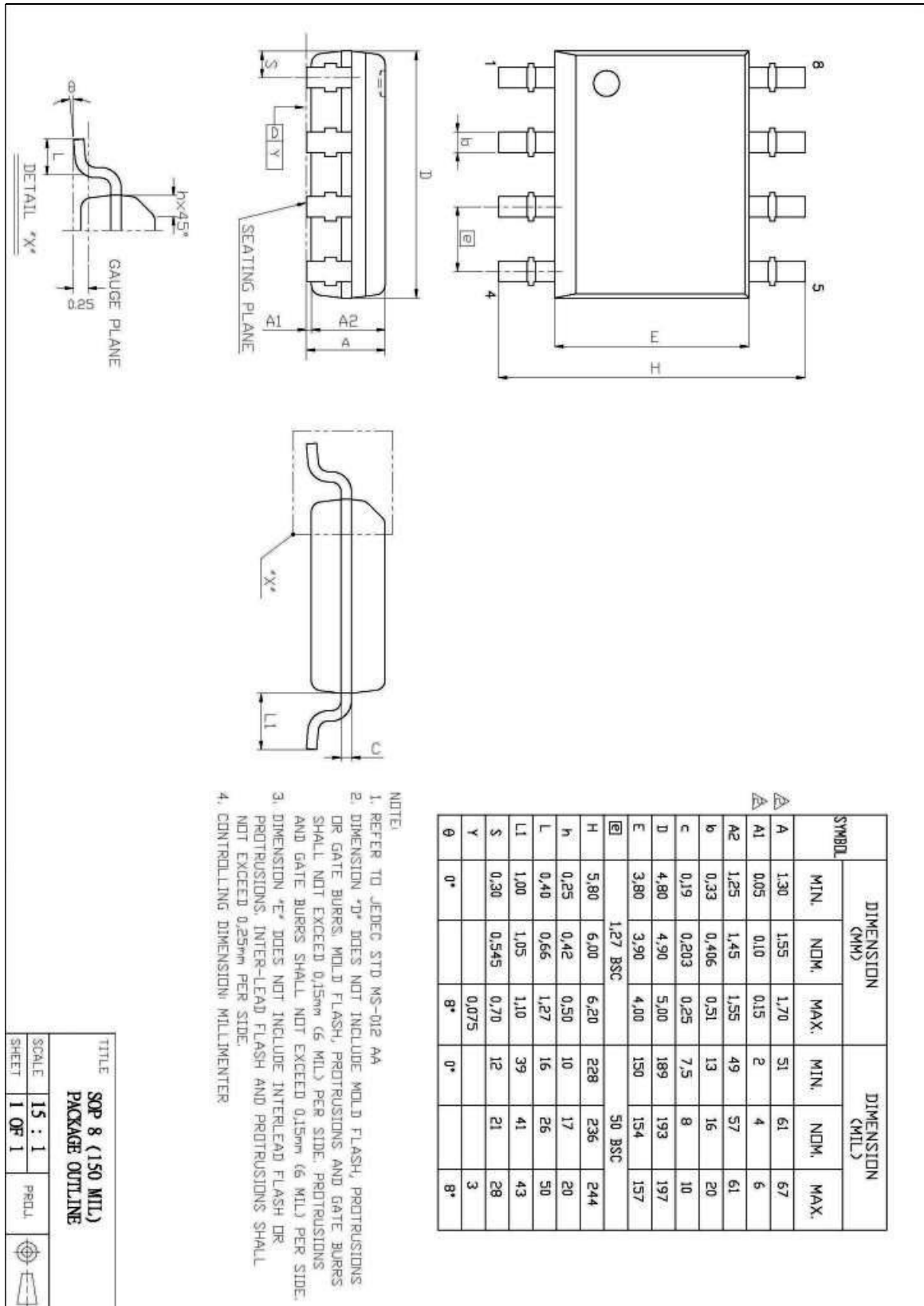


Figure 9-1 SOP8 Package Outline Diagram

10.0 Ordering Information

Table 10-1 Ordering Information

Part Number	Package Type
PL-2303SA LF	8-pin SOP Lead Free

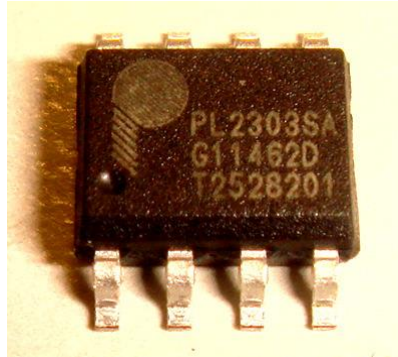


Figure 10-1 Chip Part Number Information

Table 10-2 Chip Marking Information

Line	Marking	Description
First Line	PL2303SA	Chip Product Name
Second Line (GYYWWXXX)	G	Green compound packing material (Pb-free)
	YY	Last two digits of the manufacturing year
	WW	Week number of the manufacturing year
	XXX	Chip Version (2D)
Third Line	TXXXXXXXX	Manufacturing LOT code

Example: "G11462D" – means Green packing + Year 2011 + Week no. 46 + 2D chip version.