PL2523 USB 2.0 to 2-port Full UART Controller

USB Interface

- Fully compliant with USB 2.0 specification
- USB-IF certified TID 6180
- Royalty-free USB to Virtual COM Port drivers for Windows, Mac, Linux, and Android
- UHCI/OHCI (USB1.1), EHCI (USB2.0), and xHCI (USB3) host controller compatible
- Highly integrated USB 2.0 High-Speed and Full-speed transceiver with built-in pull-up resistor and reference resistor to reduce PCB external component
- Support on-chip MTP for customization of USB device descriptor and configuration, and serial number, no need of external memory
- Each IC has unique ID (for serial number)
- Support bus-power, self-power and high-power USB configuration
- Support Windows USB selective suspend (remote wakeup enabled)
- Support VBUS detect function to attach USB host after VBUS is detected
- Support 3.3V VBUS/VIN voltage operation
- Support read-only Mass Storage Device Class for file storage.

GPIO Interface

- Versatile GPIO functions and routing logic provides easy to use multi-IO functions
- Configurable output driving strength
- Total 7 GPIOs can be used
- Optional clock output and PWM output
- HBM ±6.0KV ESD protection
- MM ±300V ESD protection
- Latch up ±200mA ESD protection

UART Interface

- Support 2-port full UART interface
  - Individual 2-port full UART interface
  - RS232, RS422, RS485
  - Up to 24Mbps flexible baud rate
  - 5, 6, 7, or 8 data bits
  - Odd, Even, Mark, Space, None parity mode
  - One, one and half, or two stop bits
  - Hardware flow control (CTS/RTS and/or DSR/DTR)
  - Software flow control (XON/XOFF)
  - Configurable remote wakeup pin
- Individual 512bytes FIFO for IN/OUT buffer per port
- Configurable threshold of flow control
- Configurable transmit and receive LED pins
- Configurable invert option of UART signals
- Suspend pin control for RS232 transceiver

Miscellaneous

- Integrated Power-on-Reset (POR) circuit
- Integrated 5V to 3.3V LDO that can support 100mA for chip internal or external components
- Independent and wide I/O voltage range (+1.8V ~ +5V) for all of 2 ports ,typical I/O voltage (1.8V/2.5V/3.3V/5V).
- Support Battery Charger (BC1.2) detection
- -40˚C to 85˚C operating temperature
- QFN48 package (RoHS compliant and Pb-free Green Compound)

Prolific Technology Inc.
7F, No.48, Sec. 3, Nan Kang Rd., Nan Kang, Taipei 115, Taiwan
Tel：+886-2-2654-6363; Fax：886-2-22654-6161
Website：http://www.prolific.com.tw/

© 2022 Prolific Inc. All rights reserved.
Proprietary and Confidential

REVISION HISTORY

Revision	Description	Date
0.1	Initial release	2022-11-7

Prolific Technology Inc.
7F, No.48, Sec. 3, Nan Kang Rd., Nan Kang, Taipei 115, Taiwan
Tel：+886-2-2654-6363; Fax：886-2-22654-6161
Website：http://www.prolific.com.tw/

© 2022 Prolific Inc. All rights reserved.
Proprietary and Confidential

Product Data Sheet PL2523

1. Product Applications

- Single-chip upgrade solution for Legacy RS232 devices to USB interface
- USB to RS232/RS422/RS485 interface converters/cables/dongles/adapters
- MCU-based devices to USB host interface
- Point-of-Sale (POS) Terminals/Printers/Pole Displays
- USB Barcode/Smart Card Readers
- PC I/O Docking Station/Port Replicators
- Healthcare/Medical USB Interface Data Transfer Cable
- Serial-over-IP Wireless Solution
- Cellular/PDA USB Interface Data Transfer Cable
- GPS/Navigation USB Interface
- Industrial / Instrumentation / Automation Control USB Interface
- USB Modem / Wireless / Zigbee USB Interface
- Set-Top Box (STB) / Home Gateway USB Interface
- Battery Charger Detection for high-current and quick charging of batteries.

2. Royalty-Free Driver Support

- Windows 11, 10, 8, 7 (Microsoft Certified WHQL Drivers)
- Windows Server 2008 R2, 2012, 2016, 2019, 2022
- Mac OS X
- Linux OS
- Android 3.2 and above

3. Ordering Information

Chip Product Name	Package Type	Ordering Part Number	MPQ
PL2523	48-pin QFN (7x7mm)	PL2523A2FMG7P1	260pcs / tray
		PL2523A2FMG8P1	2000pcs / reel

Prolific Technology Inc.
7F, No.48, Sec. 3, Nan Kang Rd., Nan Kang, Taipei 115, Taiwan
Tel：+886-2-2654-6363; Fax：886-2-22654-6161
Website：http://www.prolific.com.tw/

© 2022 Prolific Inc. All rights reserved.
Proprietary and Confidential

4. Block Diagram

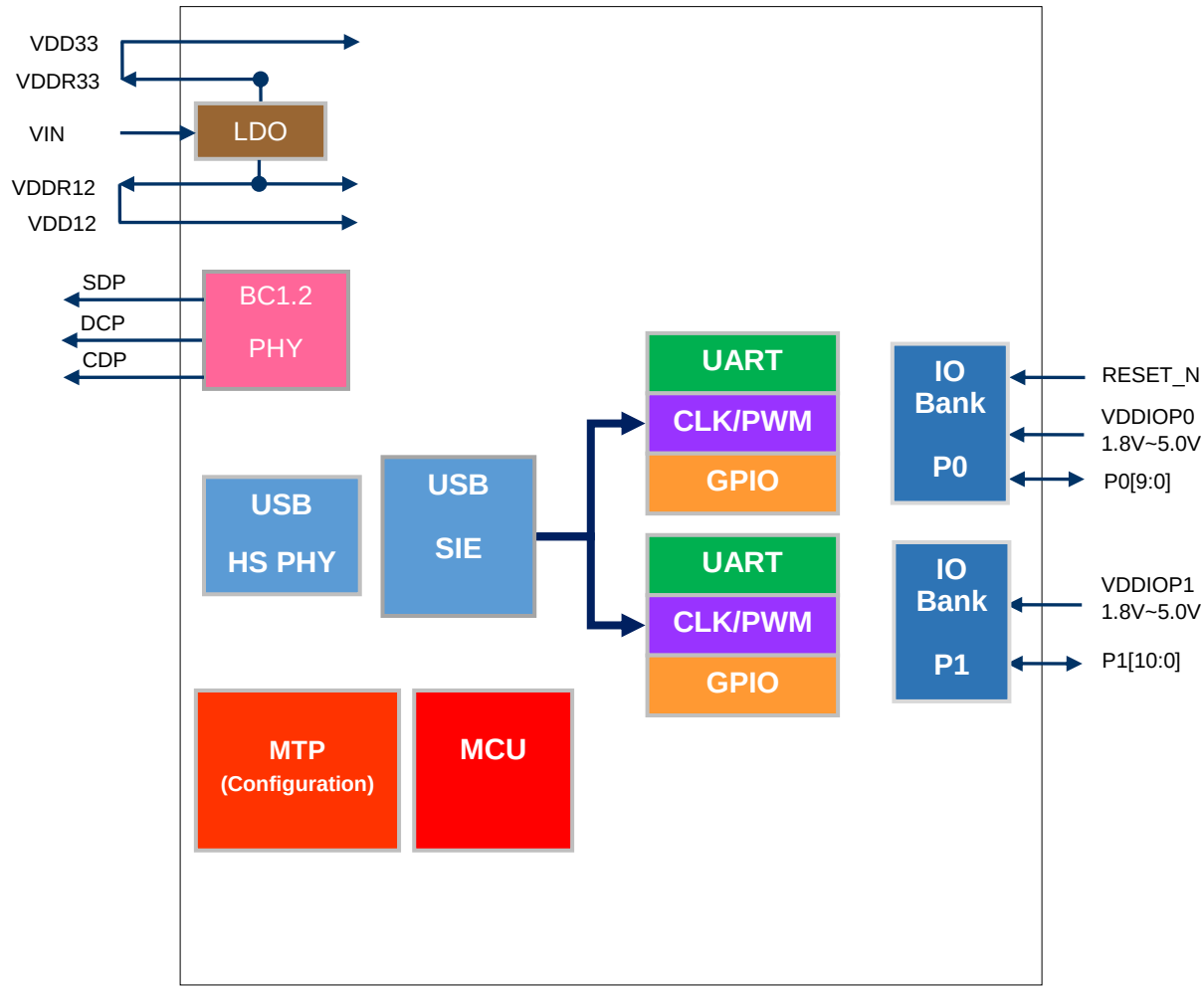


Figure 4-1: PL2523 Block Diagram

© 2022 Prolific Inc. All rights reserved.
Proprietary and Confidential

5. USB Logo Certification

The PL2523 IC has been certified by the USB-IF organization with TID 6180 to be fully compliant with the USB 2.0 specification.

Prolific Technology Inc.
7F, No.48, Sec. 3, Nan Kang Rd., Nan Kang, Taipei 115, Taiwan
Tel：+886-2-2654-6363; Fax：886-2-22654-6161
Website：http://www.prolific.com.tw/

© 2022 Prolific Inc. All rights reserved.
Proprietary and Confidential

Table of Contents

List of Figures

List of Tables

6. Overview

The new PL2523 chip provides an advanced full-featured single-chip bridge solution for connecting 2 COM port full-duplex UART asynchronous serial interface device to any Universal Serial Bus (USB) capable host. The PL2523 provides highly compatible USB drivers to simulate the traditional COM port (via virtual COM Port) on most popular operating systems and to allow existing serial UART applications based on legacy COM port.

The PL2523 also integrates an USB 2.0 transceiver, Serial Interface Engine (SIE), LDO voltage regulator, power-on- reset (POR), FIFO data buffers, and MTPROM.

PL2523 includes several new features and enhancements:

- New USB drivers for different OS platforms with faster performance and advanced features.
- Precise baud rate generator (up to 24Mbps).
- MTPROM can be programmed directly through USB (no high voltage generator required).
- Individual 512bytes FIFO for IN/OUT buffer per port
- Up to 7configurable GPIO pins.
- Versatile GPIO functions and routing logic (TX/RX LED, VBUS_DET, USB_CFG, CLK_OUT, etc.).
- Support 3.3V VBUS/VIN voltage operation.
- Wide I/O voltage range (1.8V/2.5V/3.3V/5V).
- Configurable I/O pin output driving strength.
- UART inverted signal configurable option.
- Unique USB Serial Number for each IC.
- Support Battery Charger (BC1.2) Detection to enable fast charging of batteries.

PL2523 also implements a read-only USB Mass Storage Device (CDROM) with external SPI flash memory to store driver, user files and program. This feature allows the end-product to be environmental-friendly and cost-effective.

The PL2523 is available in 48-pin QFN package with Pb-free (RoHS compliant) green package.

7. Pin Assignment & Description

7.1 PL2523 Pin Assignment

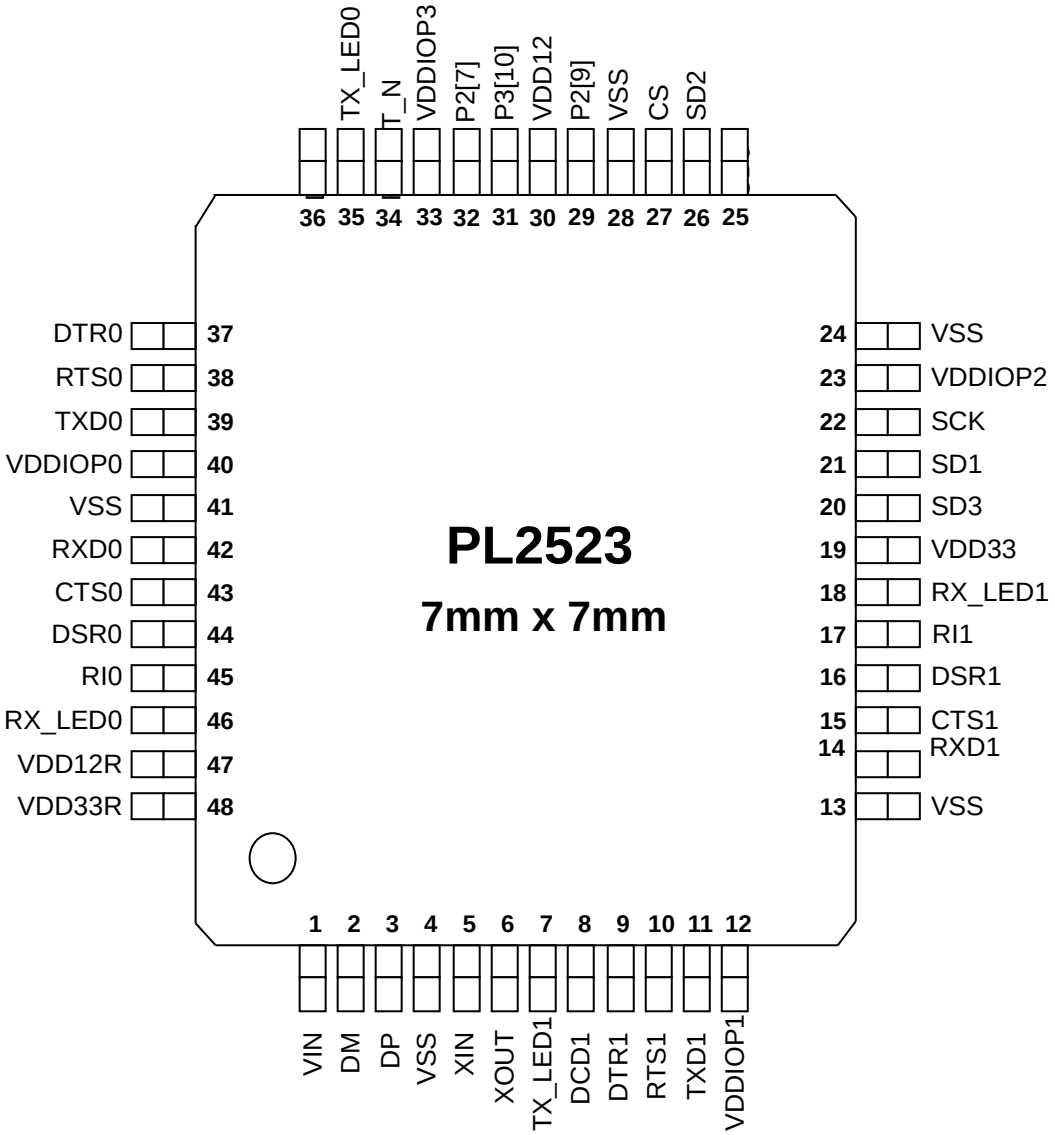


Figure 7-1: PL2523 Pin Diagram

7.2 Pin Out Description

Table 7-1: USB Data Interface Pins

Pin Name	QFN48 Pin No.	Type	Description
DP	2	I/O	USB Port Data Plus (D+) Signal.
DM	3	I/O	USB Port Data Minus (D-) Signal.

Table 7-2: UART (Serial Port) Interface Pins

Pin Name	QFN48 Pin No.	Type	Description
TXD0	39	Output	P0 Serial Port: Transmitted Data Output
DTR0	37	Output	P0 Serial Port: Data Terminal Ready Control Output
RTS0	38	Output	P0 Serial Port: Request To Send Control Output
RXD0	42	Input	P0 Serial Port: Received Data Input
RI0	45	Input	P0 Serial Port: Ring Indicator (Remote Wakeup) Control Input
DSR0	44	Input	P0 Serial Port: Data Set Ready Control Input
DCD0	36	Input	P0 Serial Port: Data Carrier Detect Control Input
CTS0	43	Input	P0 Serial Port: Clear To Send Control Input
TXD1	11	Output	P1 Serial Port: Transmitted Data Output
DTR1	9	Output	P1 Serial Port: Data Terminal Ready Control Output
RTS1	10	Output	P1 Serial Port: Request To Send Control Output
RXD1	14	Input	P1 Serial Port: Received Data Input
RI1	17	Input	P1 Serial Port: Ring Indicator (Remote Wakeup) Control Input
DSR1	16	Input	P1 Serial Port: Data Set Ready Control Input
DCD1	8	Input	P1 Serial Port: Data Carrier Detect Control Input
CTS1	15	Input	P1 Serial Port: Clear To Send Control Input

NOTE: All input pins of UART function are default pull up

Table 7-3: Configurable GPIO Pins

Pin Name	QFN48 Pin No.	Type	Description
TX_LED0	35	I/O	Configurable GPIO Pin. (see Section 7.2)
RX_LED0	46	I/O	Configurable GPIO Pin. (see Section 7.2)
TX_LED1	7	I/O	Configurable GPIO Pin. (see Section 7.2)
RX_LED1	18	I/O	Configurable GPIO Pin. (see Section 7.2)
P2[7]	32	I/O	Configurable GPIO Pin. (see Section 7.2)
P2[9]	29	I/O	Configurable GPIO Pin. (see Section 7.2)
P3[10]	31	I/O	Configurable GPIO Pin. (see Section 7.2)

NOTE: All GPIO pins are default Input mode

Table 7-4: SPI interface Pins

Pin Name	QFN48 Pin No.	Type	Description
SD0	25	I/O	SPI Data 0
SD1	21	I/O	SPI Data 1

SD2	26	I/O	SPI Data 2
SD3	20	I/O	SPI Data 3
CS	27	Output	SPI Chip Select
SCK	22	Output	SPI Clock

Table 7-5: Power and Ground Pins

Pin Name	QFN48 Pin No.	Type	Description
VDDIOP0	40	Power	+1.8V to +5V P0 I/O signal power input pin. **Note: VDD_IO voltage should not be larger than VIN voltage.**
VDDIOP1	12	Power	+1.8V to +5V P1 I/O signal power input pin.
VDDIOP2	23	Power	+1.8V to +5V P2 I/O signal power input pin.
VDDIOP3	33	Power	+1.8V to +5V P3 I/O signal power input pin.
VDD33R	48	Power	+3.3V LDO regulator output. For self-powered design, supply +3.3V to this pin.
VDD12R	47	Power	+1.2V LDO regulator output. **Note: Shall not be used for supplying external other circuits.**
VDD33	19	Power	+3.3V Power input
VDD12	30	Power	+1.2V Power input
VSS	4, 13, 24, 28,41,49(Exposed Pad)	Power	Ground
VIN	1	Power	LDO regulator input. Supply power of +3.3V - +5.25V

Table 7-6: Miscellaneous Pins

Pin Name	QFN48 Pin No.	Type	Description
RESET_N	34	Input	Active low external reset pin input is used to reset the PL2523. NOTE: This pin is internal pulled high.
XI	5	Input	12MHz crystal oscillator input.
XOUT	6	Output	12MHz crystal oscillator output.

7.3 GPIO Multi- Function Options

The PL2523 chip (QFN48 package) provides a total of 7 configurable GPIO (General Purpose I/O) pins. The pins are grouped into P0 and P1 set of pins. The table below shows the possible functions that can be configured for each GPIO pin. These special functions can be easily configured in the MTPROM of the PL2523 using the Prolific MTPROM software tool. When these pins are configured as standard GPIO pins, customers can refer to the Prolific GPIO SDK (software development kit) to develop software to control the GPIO pins for desired functions in customer application.

Table 7-7: Configurable GPIO Multi-Function Pins

GPIO	QFN48 Pin No.	Factory Default	Configurable Options (using MTP Tool)			
P0[0]	39	TXD0				
P0[1]	42	RXD0				
P0[2]	38	RTS0				
P0[3]	43	CTS0				
P0[4]	37	DTR0				
P0[5]	44	DSR0	PWMB0			
P0[6]	36	DCD0	PWMA0			
P0[7]	45	RI0 (WAKEUP)				
P0[8]	35	TX_LED0	**GPIO**	TX_EN0	CLK0	
P0[9]	46	RX_LED0	**GPIO**	TRX_LED0	CLK0	BC_DET
P0[10]	34	External RESETB				
P1[0]	11	TXD1				
P1[1]	14	RXD1				
P1[2]	10	RTS1				
P1[3]	15	CTS1				
P1[4]	9	DTR1				
P1[5]	16	DSR1	PWMB1			
P1[6]	8	DCD1	PWMA1			
P1[7]	17	RI1 (WAKEUP)				
P1[8]	7	TX_LED1	**GPIO**	TX_EN1	CLK1	
P1[9]	18	RX_LED1	**GPIO**	TRX_LED1	CLK1	BC_SUSP_N[1]
P2[7]	32	**GPIO**	VBUS_DET			
P2[9]	29	**GPIO**	CLK2	USB_CFG_N		
P3[10]	31	SUSPEND_N	**GPIO**			

Note :

1. BC_SUSP_N = (SUSPEND_N | BC_DET)
2. There are some different special functions (BC_SUSP_N, BC_DET, SUSPEND_N, VBUS_DET, USB_CFG_N). Positive and negative functions are treated as different functions. For example, SUSPEND and SUSPEND_N are different functions.
3. Though multiple location candidates, each special function can only be assigned to one location (pin).

Table 7-8: GPIO Multi-Function Option Descriptions

GPIO Function	QFN48 GPIO Pins	Type	Description
TX_LED [0:1]	P0[8] (Pin 35) P1[8] (Pin 7)	Output	Serial Port: TXD [0:1] Access LED during transmitting data.
RX_LED [0:1]	P0[9] (Pin46) P1[9] (Pin18)	Output	Serial Port: RXD [0:1] Access LED during receiving data.
TRX_LED [0:1]	P0[9] (Pin46) P1[9] (Pin18)	Output	Serial Port: TXD [0:1]/RXD[0:1] Access LED during transmitting or receiving data.
VBUS_DET	P2[7](Pin32)?	Input	When this pin is set to VBUS_DET mode, the device will not attach to USB until VBUS_DET input pin goes to high level. There must be only one pin configured as VBUS_DET pin. Refer above note for this special function.
USB_CFG_N	P2[9] (Pin29)	Output	This active low signal is used to indicate USB device has been attached and configured by USB host. So system may detect this pin to enable function after USB configuration. Refer to above note for this special function.
TX_EN [0:1]	P0[8] (Pin 35) P1[8] (Pin 7)	Output	Transmit Data Enable Pin can be used to enable RS485/RS422 transceiver when data is being transmitted.
SUSPEND_N	P3[10] (Pin31)	Output	Active low shutdown control pin during chip is suspended. This pin is used to indicate chip entering suspend state when USB bus in suspend state. Refer to above note for this special function.
WAKEUP	P0[7] (Pin 45) P1[7] (Pin 17)	Input	The remote wakeup function is to wake up chip from suspended state when this pin is triggered in suspend state. There must be only one pin configured as WAKEUP pin. The factory default is RI[0:1] .
BC_DET	P0[9] (Pin46)	Output	Battery Charge Detect pin. This active high pin indicates BC 1.2 DCP/CDP is detected.
BC_SUSP_N	P1[9] (Pin18)	Output	This pin has same function as SUSPEND pin only if BC function is enabled and detected.
CLK [0:1]	P0[8] (Pin 35) P0[9] (Pin46) P1[8] (Pin 7) P1[9] (Pin18)	Output	Each channel has an independent clock output for external application. CLK[n] output pin can be configured to Pn[8] or Pn[9]. The n is channel number. This pin can generate clock output up to 12MHz. Clock rates can be configured in OTPROM/EEPROM or customized driver .
PWMA	P0[6] (Pin36)		There are 2 independent PWMA/PWMB

[0:1]	P1[6] (Pin8)		module in one channel. Functional description as below : Duty of PWM is HIGH:LOW = PWM0DUTY:(256 – PWM0DUTY) PWM1 period = (512 * PWM1PERIOD) base clock period, base clock is configurable by register. Duty and period also are configurable by register. Set 0x00/0xFF will turn off PWM.
PWMB [0:1]	P0[5] (Pin44) P1[5] (Pin16)		Duty of PWM is HIGH:LOW = PWM0DUTY:(256 – PWM0DUTY) PWM1 period = (512 * PWM1PERIOD) base clock period, base clock is configurable by register. Duty and period also are configurable by register. Set 0x00/0xFF will turn off PWM.

8. Functional description

8.1 BC 1.2 Detection

This function is used to detect VBUS power supply capability of USB host port and provides charging control to battery charging IC. This function is enabled in MTPROM by setting GPIO pin to BC_DET option. This pin will indicate if BC 1.2 DCP/CDP is detected when device is attached to the USB port. The external battery charging IC uses the USB_CFG and SUSP_N signal pins to control its charging current support or the BC_DET signal pin to enable fast charging current mode.

8.2 USB 2.0 HS Transceiver

The USB Transceiver provides the USB high/full-speed electrical signal requirements and USB physical interface (DP/DM). This block includes the internal USB series termination resistors on the USB data lines and pull-up resistor for the DP signal. And the R_{REF} (resistor for reference power) also is included to save BOM cost.

8.3 LDO Regulator

This block is the 5V to 3.3V and 1.2V LDO regulator to power and drive the USB transceiver. It also includes 3.3V brownout detection output signals that will be used by digital circuit to reset the chip. The LDO 5V to 3.3V can supply 100mA for chip internal and external components.

8.4 USB HS/FS SIE

The USB High/Full-Speed Serial Interface Engine (SIE) block performs the processing of USB DP/DM signals. It translates the internal parallel data to serial data and outputs to USB HS/FS transceiver to generate external USB DP/DM signals timing. It also translates external USB DP/DM signals pass through USB HS/FS transceiver to parallel data for internal circuit. This block includes 15 IN/OUT endpoints. So there are sufficient multi interfaces supported by PL2523. Using these endpoints, it can implement multi functions in a single chip.

8.5 MCU

There is a MCU inside to handle USB standard requests and vendor requests. Many different configurations can be applied if different settings is configured in MTP. The MCU will depend on the value in MTP to do related setting for different implementation.

8.6 Internal MTPROM

The MTPROM (Multi-Time Programming Memory) is used as MCU firmware and chip function settings, GPIO pin function setting and USB descriptor related data. There is 768 bytes user programming area available for customization settings. This user programming area can be easily programmed by the Prolific MTPROM software through USB port without any additional voltage converter requirement.

8.7 UART Control

There are 2 UART control modules handle the data transfer according to RS232 format and interface. Each module has full flow control, including hardware RTS/CTS, DTR/DSR and software flow control. So it can support RS232, PS485, modem etc. The IO voltage level supports wild range from 1.8 to 5.0 V. Baud rate also supports wild range from 5Hz to 24MHz and these baud rate setting is easily set by popular terminal tool through USB command.

8.8 IO Functions

The IO Functions block implements generic GPIO function and many configurable I/O functions such as TX access LED and RX access LED features, clock output features with PWM, and others.

8.9 IO Routing Logic

The PL2523 has many versatile I/O functions. Each GPIO pin includes multiple functions that can be configured in the MTPROM. This module multiplexes I/O functions to different chip I/O pins. It also handles I/O pin polarity, open-drain, pull-up/pull-down, and I/O pin drive capability functions.

9. AC & DC Characteristics

9.1 Absolute Maximum Ratings

Table 9-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{VIN}	Power supply of VIN	-0.3 to 5.5	V
V_{DD12}	Power supply of VDD12	-0.3 to 1.3	V
V_{DD33}	Power supply of VDD33	-0.3 to 3.6	V
$V_{VDDIOP0}$	Power supply of VDDIOP0	+1.8 to V_{VIN}[1]	V
$V_{VDDIOP1}$	Power supply of VDDIOP1	+1.8 to V_{VIN}[1]	V
$V_{VDDIOP2}$	Power supply of VDDIOP2	+1.8 to V_{VIN}[1]	V
$V_{VDDIOP3}$	Power supply of VDDIOP3	+1.8 to V_{VIN}[1]	V
V_{INIOP0}	Input voltage of IO of P0	-0.3 to V_{VIN}[1]	V
V_{INIOP1}	Input voltage of IO of P1	-0.3 to V_{VIN}[1]	V
V_{INIOP2}	Input voltage of IO of P2	-0.3 to V_{VIN}[1]	V
V_{INIOP3}	Input voltage of IO of P3	-0.3 to V_{VIN}[1]	V
V_{ESDHBM}	ESD HBM	6.0	KV
V_{ESDMM}	ESD MM	300	V
$I_{LATCHUP}$	Latch-up current	200	mA
T_{OP}	Operation temperature	-40 to 85	°C
T_{STG}	Storage temperature	-40 to 150	°C

1: shall not be higher than V_{VIN}

9.2 Operating Current

Table 9-2: Operating Current Parameters

Symbol	Parameter	Min	Typ	Max	Units
I_{VIN}	Current consumption of power supply of VIN. Testing condition → 1. bus power mode : power supply by USB VBUS 2. 2 ports operate concurrently without LED/transceiver @ 115200 baud rate.		37.7		mA
I_{SUS}	Suspend current		760		uA

9.3 Recommended Operating Conditions

Table 9-3: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{VIN}	Power supply of VDD50	3.3		5.25	V
V_{DD12}	Power supply of VDD12	1.1	1.2	1.3	V
V_{DD33}	Power supply of VDD33	3.0	3.3	3.6	V
$V_{VDDIOP0}$	Power supply of VDDIOP0	1.8		V_{VIN}[1]	V
$V_{VDDIOP1}$	Power supply of VDDIOP1	1.8		V_{VIN}[1]	V
$V_{VDDIOP2}$	Power supply of VDDIOP2	1.8		V_{VIN}[1]	V
$V_{VDDIOP3}$	Power supply of VDDIOP3	1.8		V_{VIN}[1]	V
V_{INIOP0}	Input voltage of IO of P0	0		V_{VIN}[1]	V
V_{INIOP1}	Input voltage of IO of P1	0		V_{VIN}[1]	V
V_{INIOP2}	Input voltage of IO of P2	0		V_{VIN}[1]	V
V_{INIOP3}	Input voltage of IO of P3	0		V_{VIN}[1]	V

1: shall not be higher than V_{VIN}

9.4 IO Characteristics

Table 9-4: IO Characteristics at VDDIO=1.8V

VIN=5.0V, VDD33=3.3V, VDD12=1.2V, **VDDIO=1.8V**, T=25 °C

Symbol		Parameter	Test Condition	Min	Typ	Max	Units
VIH		Input high voltage		1.8			V
VIL		Input low voltage				0.8	V
VOH		Output high voltage	IIO <= IOH	0.9*VDDIO			V
VOL		Output low voltage	IIO <= IOL			0.1*VDDIO	V
IOH	DRV=1	Driving high current	VIO >= 0.9*VDDIO			1.8	mA
	DRV=2	Driving high current	VIO >= 0.9*VDDIO			2.1	mA
	DRV=3	Driving high current	VIO >= 0.9*VDDIO			2.3	mA
IOL	DRV=1	Driving low current	VIO <= 0.1*VDDIO			4	mA
	DRV=2	Driving low current	VIO <= 0.1*VDDIO			6	mA
	DRV=3	Driving low current	VIO <= 0.1*VDDIO			8	mA
T_{RISE}	DRV=1	Rise time	20pF loading, 10% to 90%		28		ns
	DRV=2	Rise time	20pF loading, 10% to 90%		25		ns
	DRV=3	Rise time	20pF loading, 10% to 90%		23		ns
	DRV=1	Fall time	20pF loading, 90% to 10%		0.7		ns

T_{FALL}	DRV=2	Fall time	20pF loading, 90% to 10%		0.6		ns
	DRV=3	Fall time	20pF loading, 90% to 10%		0.5		ns
F_{BAUD}	DRV=1	UART baud rate				12M	bps
	DRV=2	UART baud rate				12M	bps
	DRV=3	UART baud rate				12M	bps
R_{PULLUP}		Pull-up resistance			75.6K		Ohm
$R_{PULLDOWN}$		Pull-down resistance			72K		Ohm
I_{LEAKHI}		Input high leakage	VIO = VDDIO Pull-up/pull-down disabled		23		uA
I_{LEAKLO}		Input low leakage	VIO = 0V Pull-up/pull-down disabled		23		uA

Table 9-5: IO Characteristics at VDDIO=3.3V

VIN=5.0V, VDD33=3.3V, VDD12=1.2V, **VDDIO=3.3V**, T=25 °C

Symbol		Parameter	Test Condition	Min	Typ	Max	Units
VIH		Input high voltage		1.4			V
VIL		Input low voltage				1.3	V
VOH		Output high voltage	IIO <= IOH	0.9*VDDIO			V
VOL		Output low voltage	IIO <= IOL			0.1*VDDIO	V
IOH	DRV=1	Driving high current	VIO >= 0.9*VDDIO			11	mA
	DRV=2	Driving high current	VIO >= 0.9*VDDIO			17	mA
	DRV=3	Driving high current	VIO >= 0.9*VDDIO			22	mA
IOL	DRV=1	Driving low current	VIO <= 0.1*VDDIO			12	mA
	DRV=2	Driving low current	VIO <= 0.1*VDDIO			18	mA
	DRV=3	Driving low current	VIO <= 0.1*VDDIO			24	mA
T_{RISE}	DRV=1	Rise time	10pF loading, 10% to 90%		4		ns
	DRV=2	Rise time	10pF loading, 10% to 90%		2		ns
	DRV=3	Rise time	10pF loading, 10% to 90%		2		ns
T_{FALL}	DRV=1	Fall time	10pF loading, 90% to 10%		1		ns
	DRV=2	Fall time	10pF loading, 90% to 10%		1		ns
	DRV=3	Fall time	10pF loading, 90% to 10%		1		ns
F_{BAUD}	DRV=1	UART baud rate				24M	bps
	DRV=2	UART baud rate				24M	bps
	DRV=3	UART baud rate				24M	bps
R_{PULLUP}		Pull-up resistance			75.6K		Ohm
$R_{PULLDOWN}$		Pull-down			72K		Ohm

		resistance					
I_{LEAKHI}		Input high leakage	VIO = VDDIO Pull-up/pull-down disabled		43		uA
I_{LEAKLO}		Input low leakage	VIO = 0V Pull-up/pull-down disabled		43		uA

Table 9-6: IO Characteristics at VDDIO=5.0V

VIN=5.0V, VDD33=3.3V, VDD12=1.2V, **VDDIO=5.0V**, T=25 °C

Symbol		Parameter	Test Condition	Min	Typ	Max	Units
VIH		Input high voltage		1.5			V
VIL		Input low voltage				1.3	V
VOH		Output high voltage	IIO <= IOH	0.9*VDDIO			V
VOL		Output low voltage	IIO <= IOL			0.1*VDDIO	V
IOH	DRV=1	Driving high current	VIO >= 0.9*VDDIO			20	mA
	DRV=2	Driving high current	VIO >= 0.9*VDDIO			28	mA
	DRV=3	Driving high current	VIO >= 0.9*VDDIO			38	mA
IOL	DRV=1	Driving low current	VIO <= 0.1*VDDIO			20	mA
	DRV=2	Driving low current	VIO <= 0.1*VDDIO			28	mA
	DRV=3	Driving low current	VIO <= 0.1*VDDIO			36	mA
T_{RISE}	DRV=1	Rise time	20pF loading, 10% to 90%		2		ns
	DRV=2	Rise time	20pF loading, 10% to 90%		2		ns
	DRV=3	Rise time	20pF loading, 10% to 90%		1.5		ns
T_{FALL}	DRV=1	Fall time	20pF loading, 90% to 10%		1.5		ns
	DRV=2	Fall time	20pF loading, 90% to 10%		1.5		ns
	DRV=3	Fall time	20pF loading, 90% to 10%		1.5		ns
F_{BAUD}	DRV=1	UART baud rate				24M	bps
	DRV=2	UART baud rate				24M	bps
	DRV=3	UART baud rate				24M	bps
R_{PULLUP}		Pull-up resistance			75.6K		Ohm
$R_{PULLDOWN}$		Pull-down resistance			72K		Ohm
I_{LEAKHI}		Input high leakage	VIO = VDDIO Pull-up/pull-down disabled		65		uA
I_{LEAKLO}		Input low leakage	VIO = 0V Pull-up/pull-down disabled		65		uA

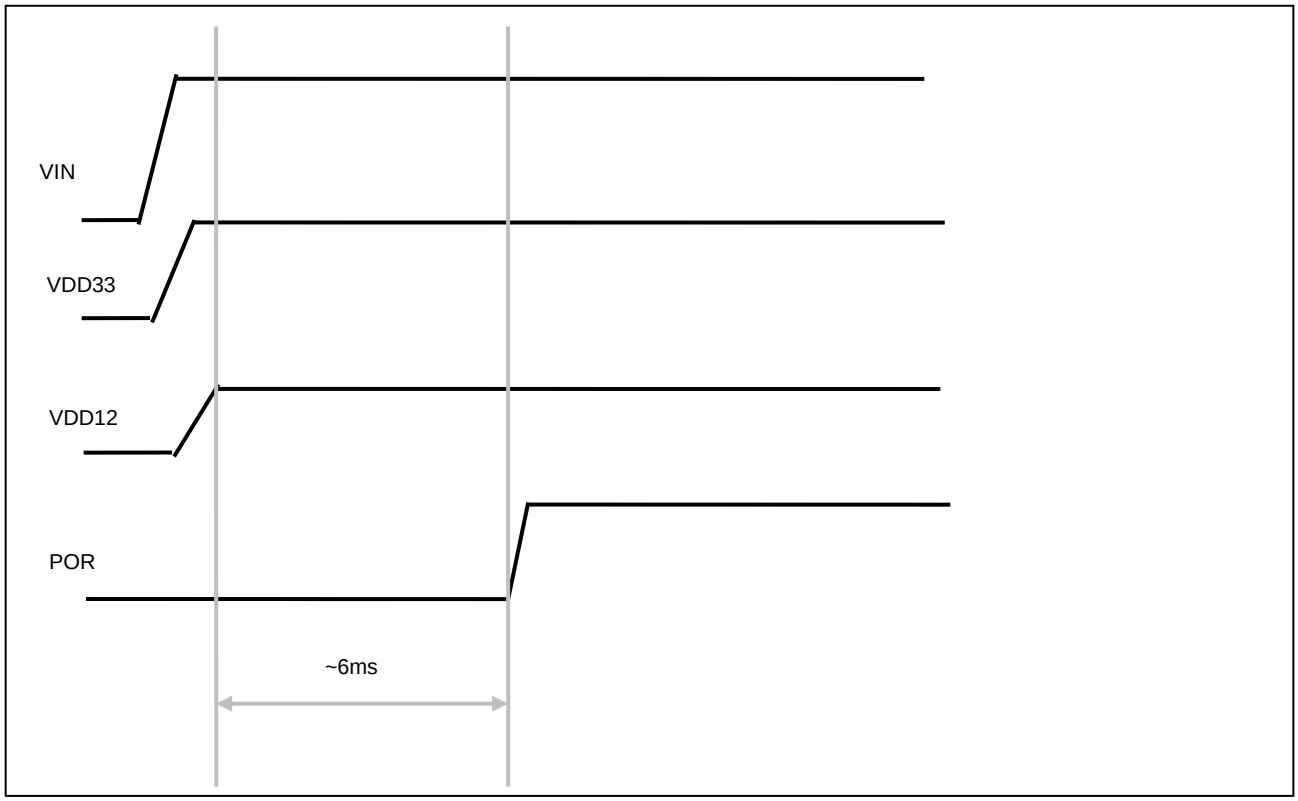
9.5 Timing parameters

Table 9-7: Timing parameters

Symbol	Parameter	Min	Typ	Max	Units
T_{POR}			6		ms

Chip Reset Control

The PL2523 has an internal power on reset circuit; therefore, external reset control circuit is optional. External reset control (RESET_N pin) can help system designs to make sure of chip operation start time.



9.6 Temperature Characteristics

Table 9-8 Temperature Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature (ambient)	--	-40	--	85	°C
Junction Operation Temperature	T_J	-40	25	125	°C

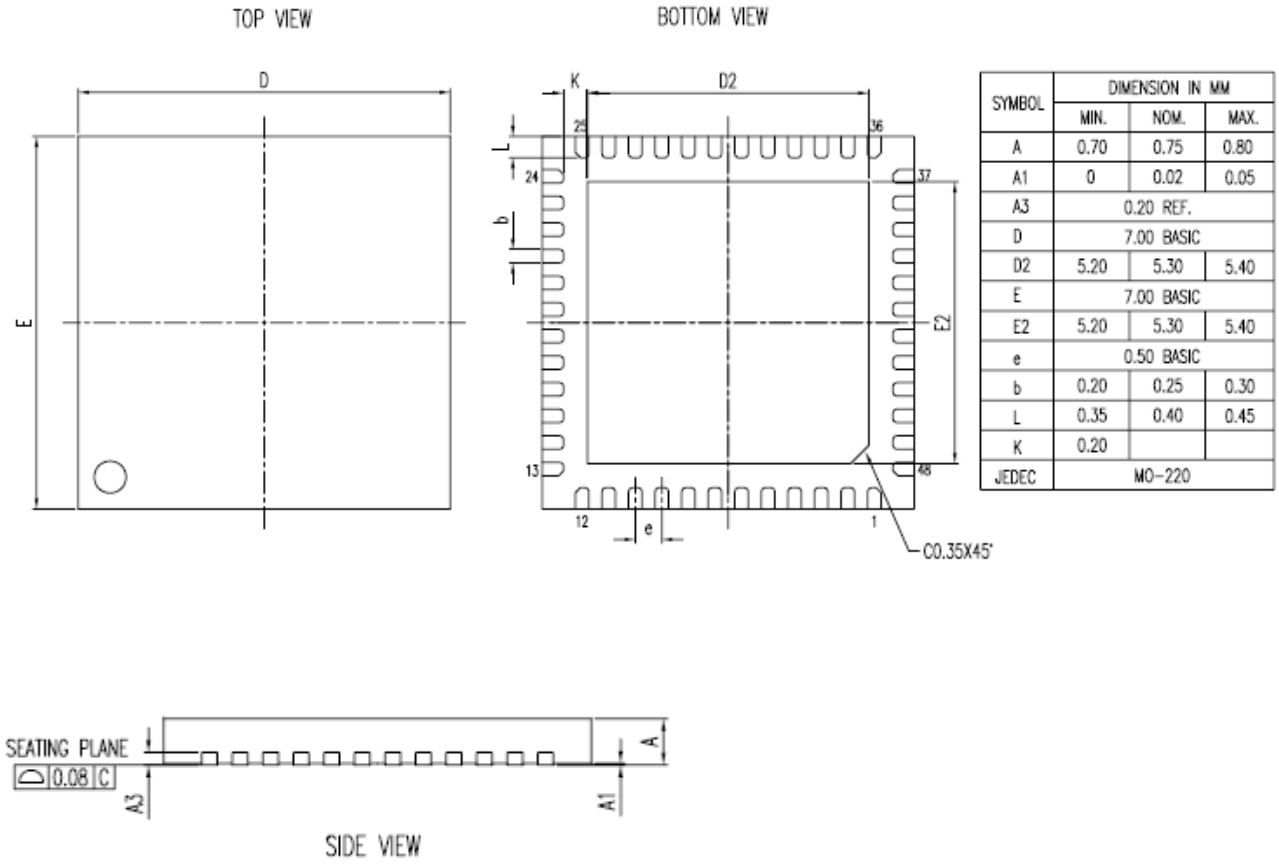
9.7 Baud Rate Characteristics

Table 9-9 Baud Rate Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Baud rate @ VDD_IO = 5V	--	5	--	24M	bps
Baud rate @ VDD_IO = 3.3V	--	5	--	24M	bps
Baud rate @ VDD_IO = 1.8V	--	5	--	12M	bps

10. Package Outline Diagram

10.1 Outline Diagram

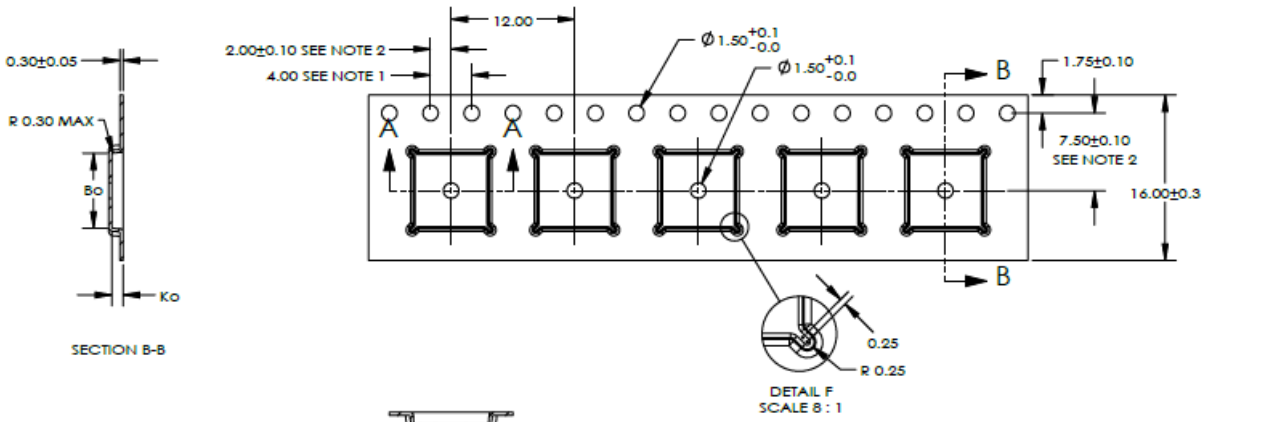


SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20 REF.	
D		7.00 BASIC	
D2	5.20	5.30	5.40
E		7.00 BASIC	
E2	5.20	5.30	5.40
e		0.50 BASIC	
b	0.20	0.25	0.30
L	0.35	0.40	0.45
K	0.20		
JEDEC		MO-220	

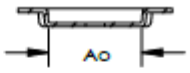
Figure 10-1: PL2523 Outline Diagram (QFN48 7x7mm)

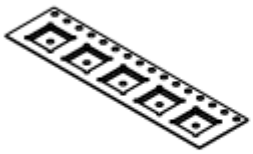
11. Package information

11.1 Carrier Tape (QFN48)



PART NUMBER	T	MATERIAL	DRAWING #
ML0707-AC	0.30	PS+C	T102533BT
ML0707-AS	0.30	PS(CLEAR)	T115504BT
ML0707-AQ	0.33	PC	T115505BT
ML0707-AD	0.30	PS+C	T115784BT





SCALE 1:1

	DIM	±
Ao	7.25	0.10
Bo	7.25	0.10
Ko	1.10	0.10

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3. Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

Disclaimer

All the information in this document is subject to change without prior notice. Prolific Technology Inc. does not make any representations or any warranties (implied or otherwise) regarding the accuracy and completeness of this document and shall in no event be liable for any loss of profit or any other commercial damage, including but not limited to special, incidental, consequential, or other damages.

Trademarks

The Prolific logo is a registered trademark of Prolific Technology Inc. All brand names and product names used in this document are trademarks or registered trademarks of their respective holders.

Copyrights

Copyright © 2022 Prolific Technology Inc. All rights reserved.

No part of this document may be reproduced or transmitted in any form by any means without the express written permission of Prolific Technology Inc.

Prolific Technology Inc.

7F, No. 48, Sec. 3, Nan Kang Rd.
Nan Kang, Taipei 115, Taiwan, R.O.C.
Telephone: +886-2-2654-6363
Fax: +886-2-2654-6161
E-mail: sales@prolific.com.tw
Website: http://www.prolific.com.tw