Application Note
PL-277x Series SuperSpeed USB 3.0 SATA Bridge Controllers PCB Layout Guide

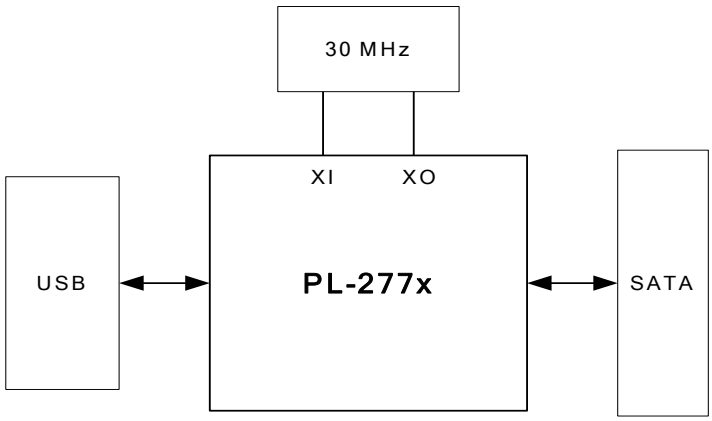
Introduction

This document explains how to design a PCB with Prolific PL-277x SuperSpeed USB 3.0 SATA Bridge Controllers. These guidelines have the following goals in mind:

1. Make a noise-free, power-stable environment suitable for the PL-277x.
2. Reduce the possibility of EMI and EMC.
3. Simplify the task of routing signal trace to make a better design circuit.

Placement Guidelines

The following are the guidelines for general routing and ideal placement:



- The distance between the USB receptacle to PL-277x should be as short as possible.
- The distance between the Crystal to PL-277x XI and XO should also be as short as possible.
- Crystal should not be placed near I/O ports, board edges, and other high-frequency devices or traces (such as Power signal) or magnetic field devices (such as magnetic).
- The outer shield of Crystal needs well grounding to prevent EMC/EMI from inducing extra noise. The retaining straps of the Crystal also need well grounding.
- High Current devices should be placed near the Power source to reduce the trace length. Traces with high current will induce more EMI.
- Do not route SATA/USB traces under crystals, oscillators, clock synthesizers, magnetic devices, or ICs that use and/or duplicate clocks.

Trace Routing

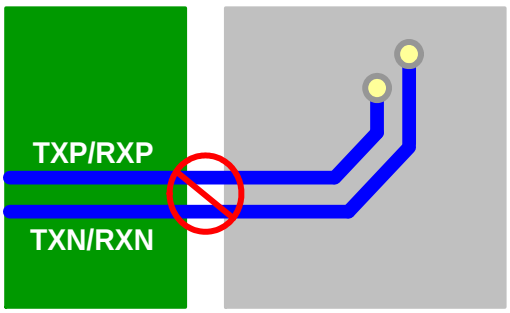
Good routing of traces can reduce the propagation delay, cross talk, and high-frequency noise. It can also improve the signal quality for the receiver and reduce the loss from transmitted signals.

- The criteria of the trace width and the spacing between the traces of a pair must be considered. Users should take the stackup, trace width, spacing between the traces of each pair, thickness of copper and paint into consideration to achieve a USB differential impedance of 90Ω. (Single ended impedance of 45Ω)

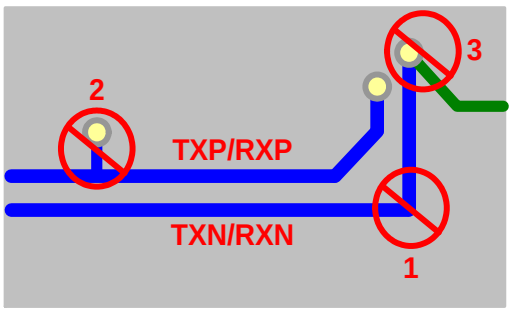
- As much as possible, wire the same equal length for USB DP/DM, SSTXP/SSTXM, SSRXP/SSRXM, TXDP/TXDN, and RXDP/RXDN. Suppress the tolerance to 1.5mm or less.

- From the viewpoints of both jitter and electromagnetic interference, the length matching is important in PCB design. The total trace skew should be less than 5 mils (recommended value) among differential pairs. The skew between the bonding wires inside the packing also affects the total skew, as does skew between the PCB traces. When designing the differential PCB traces, users should take the differences of lengths at the bonding wires into consideration.

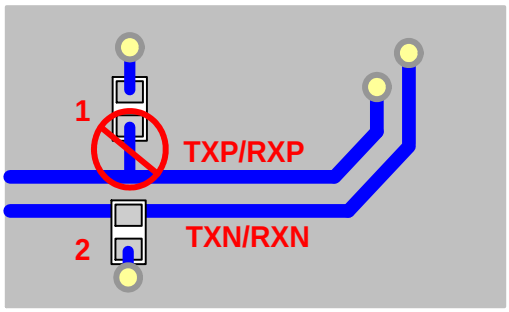
- Avoid routing to break image plane (anti-etch areas) – Route USB/SATA differential signal pair traces over continuous ground and power planes. Avoid crossing anti-etch areas or any break in the underlying planes. Don't route SATA differential signal pair trace under crystal, oscillator, clock synthesizers, magnetic devices or IC as this would cause interference.



- Avoid signal reflection – Route USB/SATA differential signal pair should not change layer by vias [see below Figure no. 3], and avoid branch trace by via [see below Figure no. 2]. These can reduce signal reflection and impedance change. If it is necessary to turn 90° [see Figure below no. 1], it is better to use two 45° turn or an arc instead of making a single 90° turn. This can reduce reflection on the signal by minimizing impedance discontinuities.

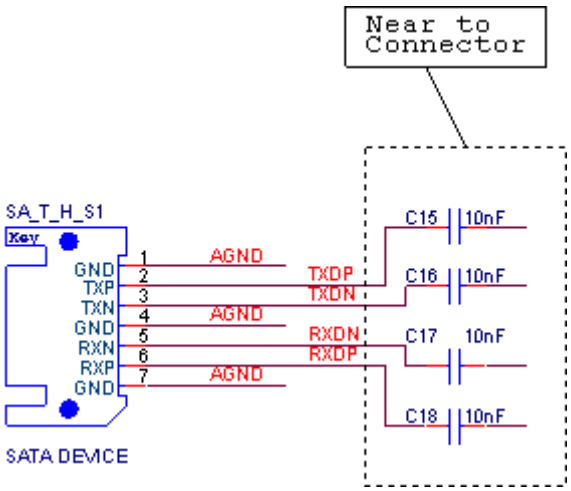


- Avoid stubs on differential pair trace – Stubs on USB/SATA differential signal pair should be avoided. While stubs exist, it will cause signal reflection and affect signal quality. If a stub is unavoidable in the design, shorten the stub length as much as possible. The sum of all stubs on a given data line should not be greater than 200 mils.



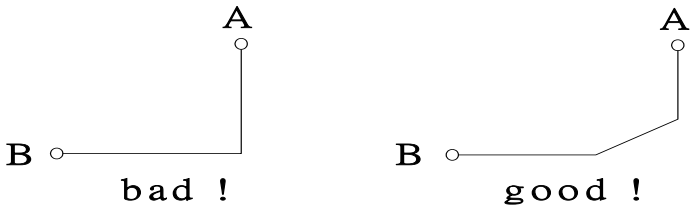
Ground Plane

- The capacitors located within the TXDP/RXDP and TXDN/RXDN path should be close to the SATA connector as much as possible.



- The capacitors located within the SSTXP/SSTXM path should be near the PL-277x chip as much as possible.
- The four trace lengths of TXDP/RXDP/TXDN/RXDN should be equal or less than 630 mil if possible.
- Spaces between TX and RX should be larger than 35 mil.
- 19 mil space between TXP and TXN is preferred but 12mil is acceptable.
- 19 mil space between RXP and RXN is preferred but 12mil is acceptable.
- Recommend test board should consist of differential traces (95Ω optimized value) over a ground plane (single ended 47.5Ω).
- Total length of differential trace (IC pad to USB receptacle through hold) should not exceed 8000 mils.

- Avoid digital signals that interfere with analog signals (crystal clock) and Power trace.
- Avoid right angle signal traces:



- The trace length and the ratio of trace width to trace height above the ground planes should be considered carefully. The clocks and other high speed signal traces should be as short and wide as possible (compare with normal digital trace). It is better to have a ground plane under these traces, and if possible, with GND plane around.
- The trace length between crystal and crystal oscillator input pin, and the trace length between crystal and crystal oscillator output pin should be equal.
- The traces listed below should be wider and short as possible. The traces should also not cross any signal traces.
    - The traces between the crystal and PL277x crystal oscillator input/output pins.
    - The traces between USB receptacle and DM, DP, SSRXP, SSRXM, SSTXP, SSTXM.
    - The traces between the capacitors and the regulator input, output, and ground.
- Route SATA/USB signals ground referenced.
- Route SATA /USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes. Use a maximum of 2 vias per trace. Vias should be matched on traces within a transmit or receive pair.
- Minimize the length of clock and periodic signal traces that run parallel to SATA/USB signal lines to minimize crosstalk. The minimum recommended spacing to clock signals is 50 mils.
- Use 20-mil minimum spacing between SATA/USB signal pairs and other signal traces. This helps to prevent crosstalk.

Design of Via

- The distances between the vias should be kept as apart as much as possible.
- The traces of differential pairs should have at least two vias and should avoid more than two.
- Two traces in differential pair should have identical number of vias and should have identical bounding pad shape and size.
- Through-hole via should be avoided as much as possible. There should be enough space between the through-hole and the adjacent metal on the PCB.

Power and Ground Planes

- Power plane: support PL-277x and other devices. Avoid using unnecessary power trace to PL-277x and keep these traces short and wide.
- GND plane - You can separate the digital GND to Analog GND as follows: Partition of GND plane needs experience and experiment. The key point is to keep the return path of analog GND almost the same to the common GND. If you do not feel confident on this, simply leave the GND plane unchanged (i.e. no partition at all).
- For all partition on Power/GND plane, right angle is not recommended. This is the same to the signal/power/bus traces.
- RREF: Connect to 12KΩ accurate resistor. Place the resistor as close as possible to chip and as possible same layer with USB chip. Avoid any toggle signal.
- Keep the net of RREF away from any signal with high-speed clocks/periodic and avoid any Via.
- Allow a minimum spacing of 2mm between the power trace and other signal traces.

For Better and More Stable Analog Performance

- The recommended accuracy of the crystal (30MHz) is 50 ppm or less.
- When using 30MHz crystal as clock source, you should pay more attention to the specification of crystal. Please refer to the USB crystal spec. When using crystal as specification, two matching caps (10pF in schematic) should be attached to the XI and XO pin.
- When using oscillator as clock source (30MHz), avoid attaching any cap on the clock trace.
- GND plane partition is not recommended, please keep the GND plane as large and clear as possible.
- Capacitance of 2.2 nF with low Equivalent Series Resistance (ESR) is required. Route as close as possible to the USB chip.
- AC coupling capacitors must be located at the transmitter side. Capacitance of 0.1 uF with low Equivalent Series Inductance (ESL) is recommended. Place AC coupling capacitors as close as possible to the chip. The second option is to place the AC coupling capacitors as close as possible to the USB receptacle.

Other Layout Recommendations

Following are other layout recommendations:

- With minimum trace lengths, route clock and USB differential pairs first.
- Route all traces over continuous planes (GND) with no interruptions. Avoid crossing over anti-etch if possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces.
- Keep traces at least 90 mils away from the edge of the plane (VCC or GND depending on which plane to which the trace is routed). This helps prevent the coupling of the signal onto adjacent wires and helps prevent free radiation of the signal from the edge of the PCB.
- In certain systems where a short, very low loss cable is to be exclusively used, it may be desirable to use longer trace lengths to optimize USB/SATA signal quality at the device receiver (RX connector specification). Careful simulation and/or studies on prototypes of signal quality are required to balance this trade off effectively.
- Each decoupling capacitor should be placed with one or two Vias to a voltage plane (or plane fill area) and solid ground plane.
- Crossing a split plane should be avoided as much as possible. When routing over a split plane, a discontinuity of impedance and failure return current path will occur, and it will cause reflections and EMI problems.

Disclaimer

All the information in this document is subject to change without prior notice. Prolific Technology Inc. does not make any representations or any warranties (implied or otherwise) regarding the accuracy and completeness of this document and shall in no event be liable for any loss of profit or any other commercial damage, including but not limited to special, incidental, consequential, or other damages.

Copyrights

Prolific Technology Inc.

7F, No. 48, Sec. 3, Nan Kang Road
Nan Kang, Taipei 115
Taiwan, R.O.C.

Telephone: +886-2-2654-6363
Fax: +886-2-2654-6161
Homepage: http://www.prolific.com.tw/