PL2771 SuperSpeed USB 3.0 SATA Bridge Controller

Product Datasheet

Document Revision: 1.0.2
Document Release: September 1, 2010

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Revision History

Revision	Description	Date
1.0.2	➢ Revised Section 1.3 (Target Applications) ➢ Revised Section 5.2 (Core Power Supply) ➢ Revised Section 5.5 (Suspend Current)	September 1, 2010
1.0.1	➢ Revised Section 1.2 and added Target Applications section ➢ Revised Section 5.1	July 26, 2010
1.0.0	➢ Formal version	July 7, 2010
0.9E	➢ Correct LQFP64 Pin Assignment and Description	February 3, 2010
0.9D	➢ Modified Pin Assignment and Description	January 29, 2010
0.9C	➢ Added QFN48 Package Information	December 22, 2009
0.9B	➢ Updated LQFP64 Package Information	November 27, 2009

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1.0 Product Overview

1.1 Overview

The PL2771 is a low-power single-chip SuperSpeed USB 3.0 to SATA II compliant bridge IC controller. It is designed to perform seamless protocol transfer between the USB host PC and SATA interface storage devices like Hard Disk Drives, Optical Disk Drives, and Solid-State Drives. SuperSpeed USB 3.0 has data transfer bandwidth of up to 5Gbps offering 10X performance increase over Hi-Speed USB 2.0 (480Mbps) while still retaining backward compatibility and interoperability with all USB2.0 and USB1.1 devices, hosts, and hubs. The PL2771 also integrates a high performance 8-bit microcontroller which can be used to support versatile system applications such as one button backup, power control, and other USB port features. The PL2771 chip is also implemented according to the USB Bulk-Only Mass Storage Class Specification v1.0.

1.2 Features

- High Performance USB 3.0 to SATA Storage Bridge Controller
- USB 3.0 Specification and USB 2.0 Specification Compliant
  - USB-IF SuperSpeed Logo Certified (TID No. 340000009)
  - SuperSpeed(5Gbps), Hi-Speed(480Mbps), and Full-Speed(12Mbps)
  - USB Mass Storage Class Bulk-Only Transport
- Serial ATA Revision 3.0 Specification Compliant
  - SATA Gen2i/Gen2m (3Gbps) and SATA Gen1i/Gen1m (1.5 Gbps)
  - Supports SATA Hot Plug
  - Supports SATA Port Multiplier
- Supports over 2-Terabytes and 4KB-sector Hard Drives
- Supports USB3.0/USB2.0/SATA Power Saving Management
- High Performance Embedded 8-bit Microcontroller
- Internal data buffer for downstream and upstream optimized data transfer performance
- Firmware update, Vendor/Product ID, and other related configuration information can be programmed to external Serial EEPROM or SPI serial flash through USB interface.
- Generic SPI interface and I2C interface for ICP
- 12 General Purpose IO (GPIO) pins can be defined for specific functions by external configuration ROM or through USB interface. Also provides SDK for further applications.
- Supports two PWM interfaces
- Supports single 30-MHz reference clock
- Ultra-low power 1.2V core operating voltage by 0.13um process
- Inexpensive LQFP64 and QFN48 package

1.3 Target Applications

- USB 3.0 External HDD/SSD/ODD
- Portable Media Player
- SATA Port Multiplier

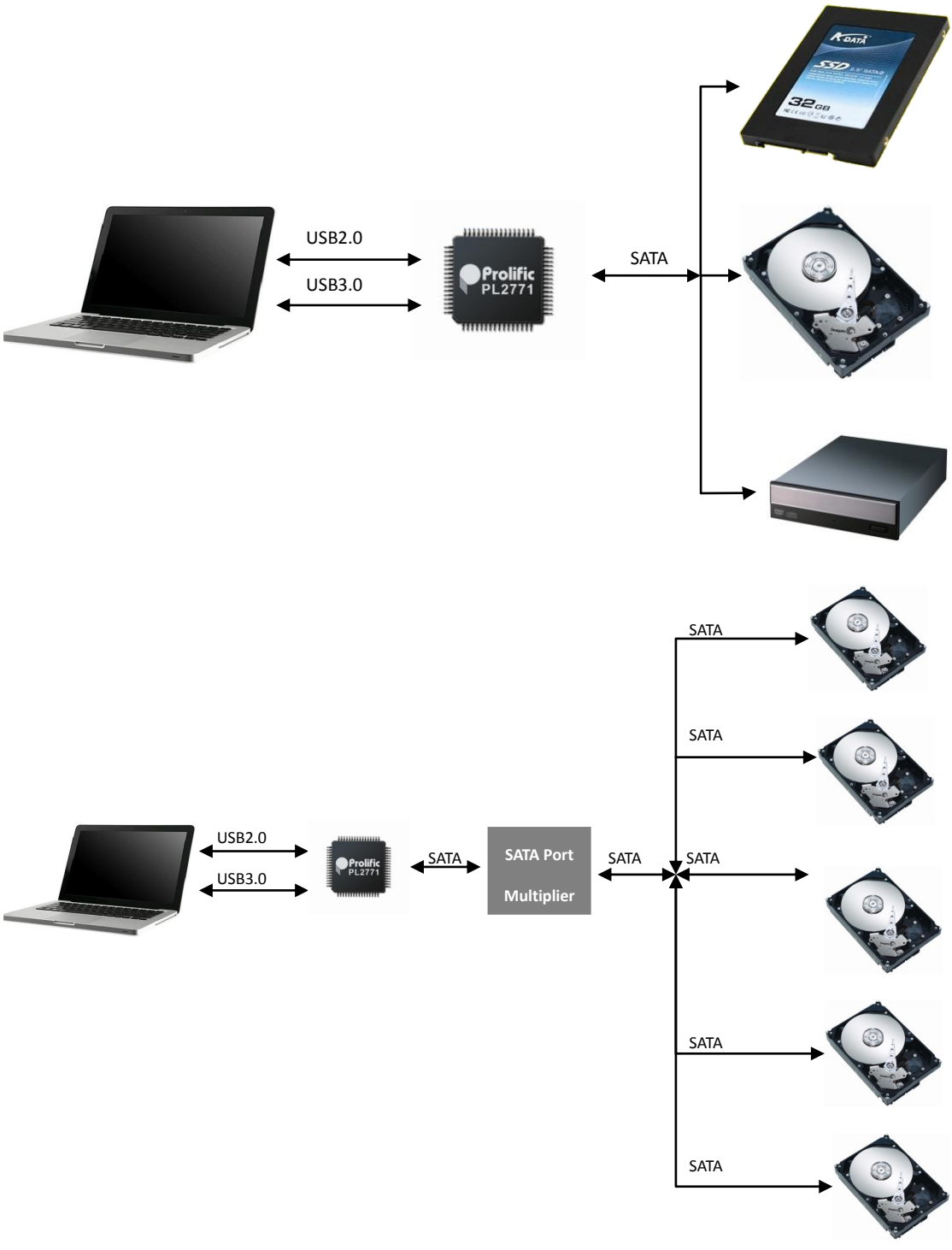


Figure 1-1 PL2771 Target Applications

1.4 Block Diagram

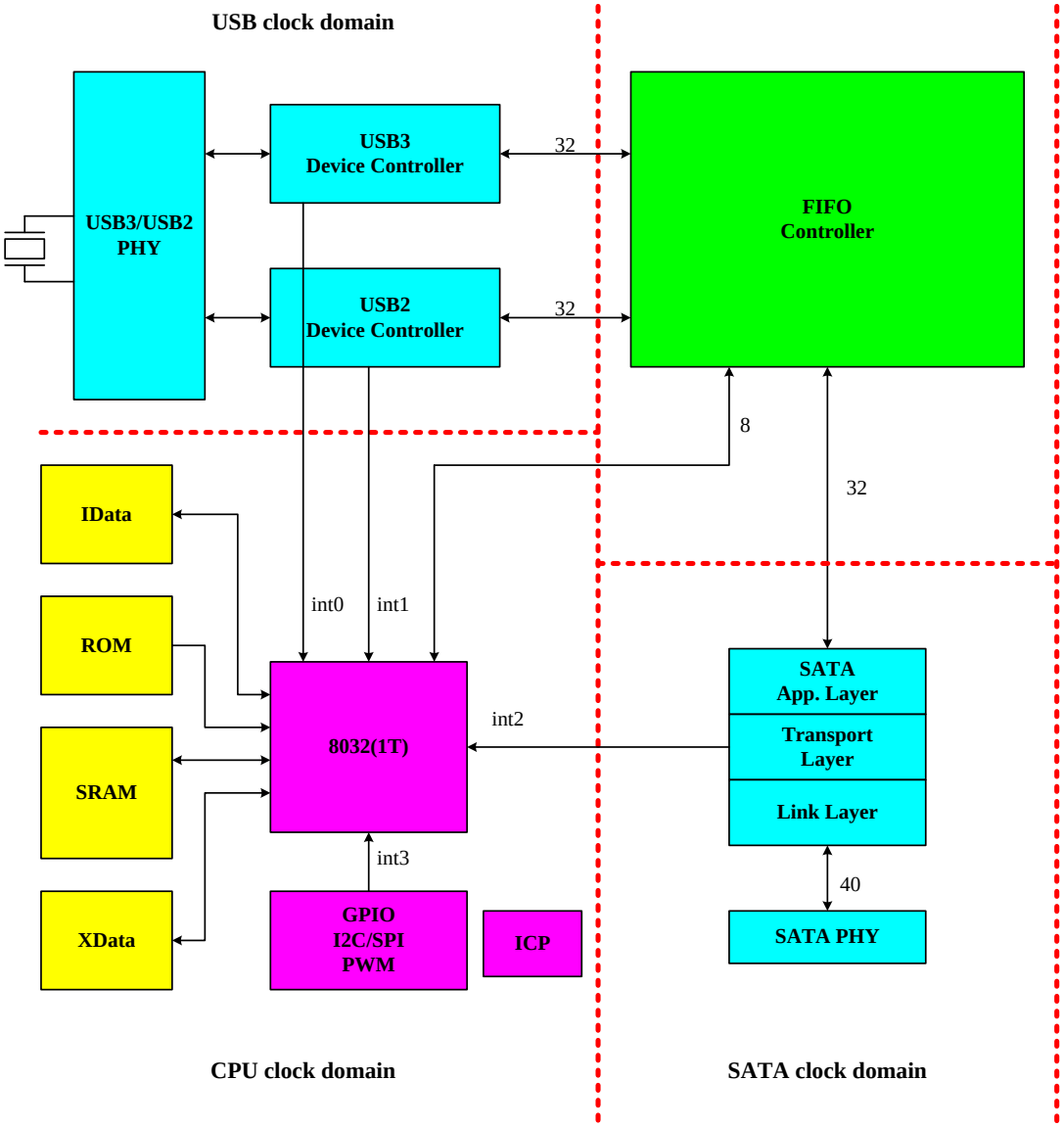


Figure 1-2 Block Diagram of PL2771

2.0 PIN Assignment Diagram

2.1 LQFP64 Pin Assignment Diagram

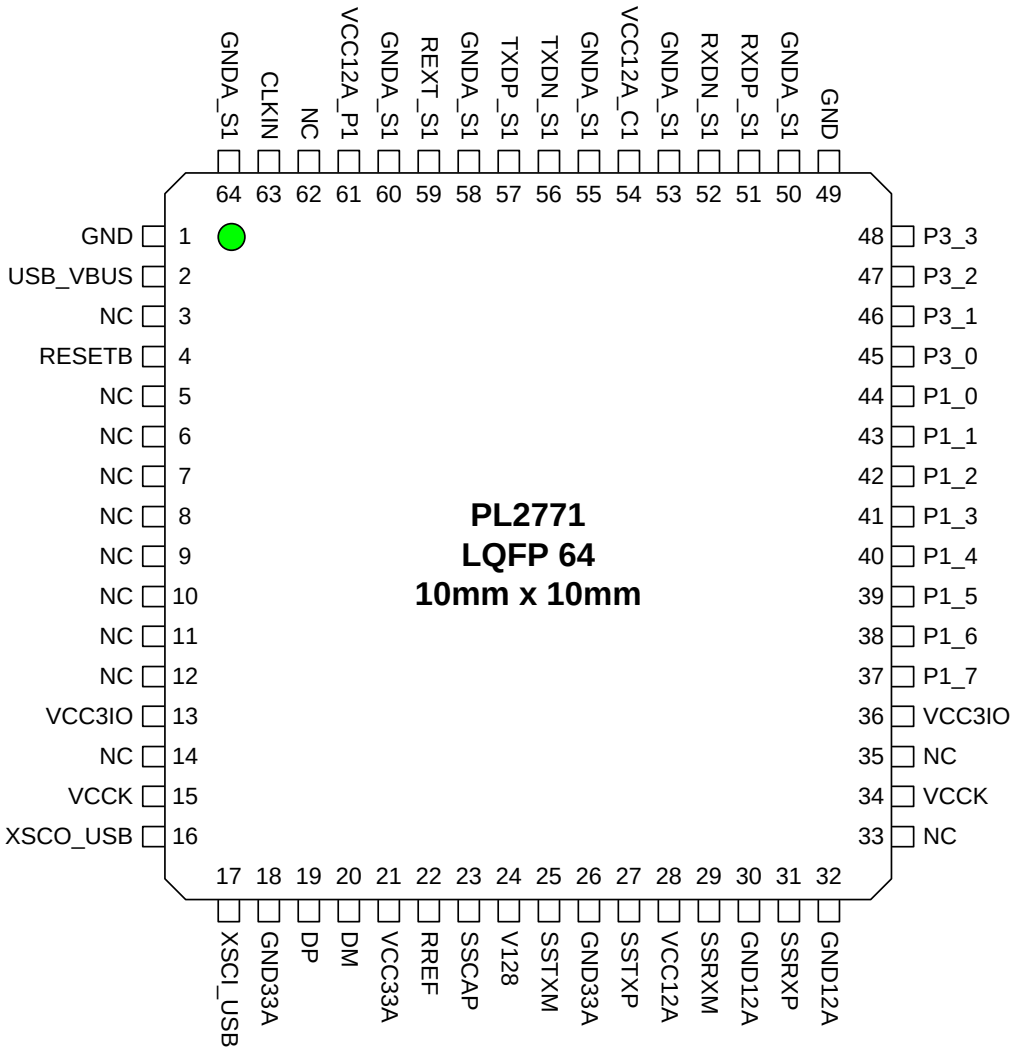


Figure 2-1 Pin Assignment Diagram of PL2771 LQFP64

2.2 QFN48 Pin Assignment Diagram

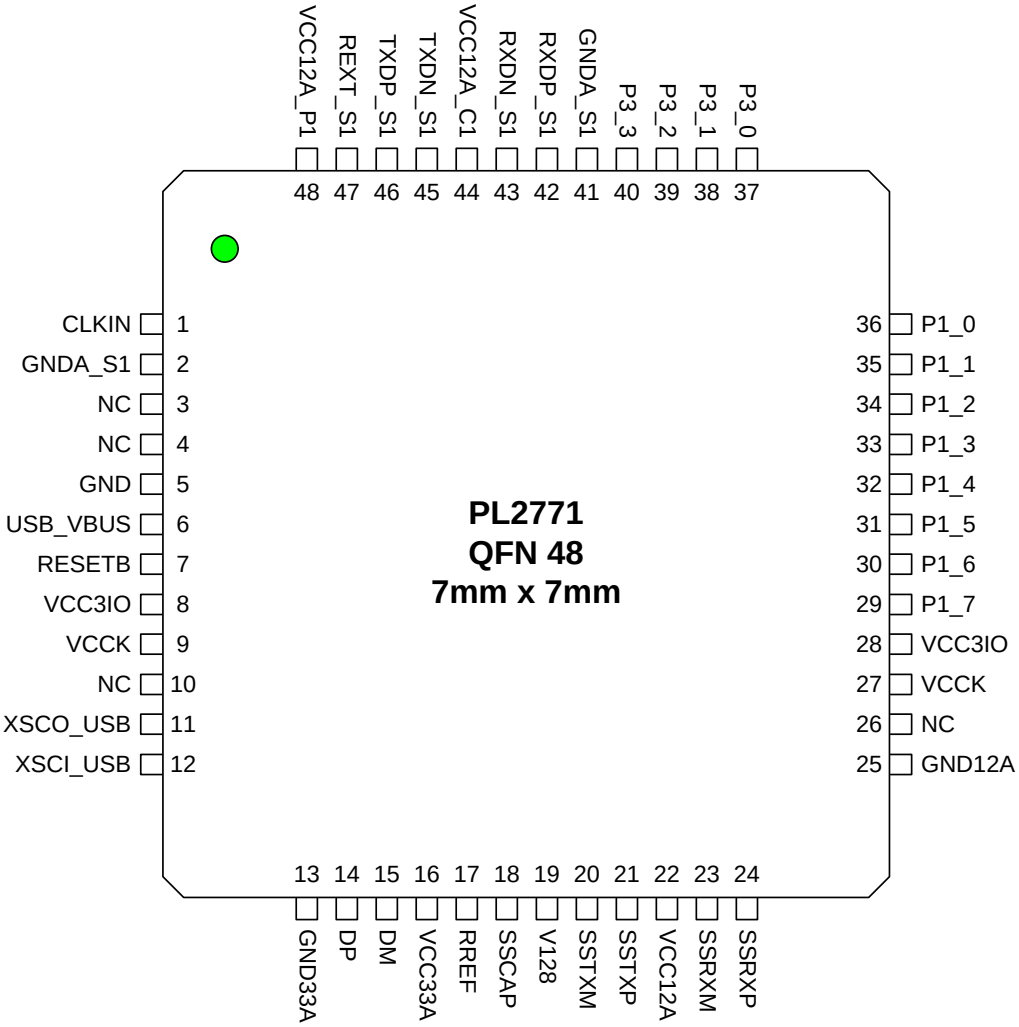


Figure 2-2 Pin Assignment Diagram of PL2771 QFN48

3.0 PIN Assignment Description

3.1 USB PHY Related Pins

Pin Type Abbreviation:

I: Input	O: Output	B: Bidirectional	A: Analog	P: Power/Ground

Table 3-1 USB2.0 PHY Related Pins

Symbol	Type	Pin No. LQFP64	Pin No. QFN48	Description
RREF	A	22	17	External resistor (12KΩ) for bias current generation
DP	B	19	14	High speed D+ signal
DM	B	20	15	High speed D- signal
XSCI_USB	I	17	12	USB Crystal oscillator input. (30MHz)
XSCO_USB	O	16	11	USB Crystal oscillator output. (30MHz)
VCC33A	P	21	16	Analog 3.3V supply voltage
GND33A	P	18,26	13	Analog ground
VCC12A	P	28	22	Analog 1.2V supply voltage.
GND12A	P	30,32	25	Analog ground
SSCAP	O	23	18	Connect an external capacitor (X7R 2.2nF ±10%) to GND33A
V128	P	24	19	Analog 1.2V supply voltage.
SSTXP	A	27	21	Differential SuperSpeed transmitting data (positive terminal)
SSTXM	A	25	20	Differential SuperSpeed transmitting data (negative terminal)
SSRXP	A	31	24	Differential SuperSpeed receiving data (positive terminal)
SSRXM	A	29	23	Differential SuperSpeed receiving data (negative terminal)

3.2 SATA PHY Related Pins

Table 3-2 SATA PHY Related Pins

Symbol	Type	Pin No. LQFP64	Pin No. QFN48	Description
GNDA_S1	P	50,53,55,58, 60,64	2,41	Analog ground
RXDP_S1	A	51	42	Receive Data (Receiver positive input)
RXDN_S1	A	52	43	Receive Data (Receiver negative input)
VCC12A_C1	P	54	44	Analog 1.2V supply voltage
VCC12A_P1	P	61	48	Analog 1.2V supply voltage
TXDN_S1	A	56	45	Transmit Data (Transmitter negative output)

TXDP_S1	A	57	46	Transmit Data (Transmitter positive output)
REXT_S1	A	59	47	External resistor (1KΩ) resistor for bias current generation.
CLKIN	I	63	1	SATA Crystal oscillator input (30MHz) NOTE: SATA PHY shares the same USB PHY crystal oscillator.

3.3 System & GPIO Pins

Table 3-3 System & GPIO Pins

Symbol	Type	Pin No. LQFP64	Pin No. QFN48	Description
VCC3IO	P	13,36	8,28	PAD power
RESETB	I	4	7	External Reset pin (Active low: Schmitt-trigger)
USB_VBUS	I	2	6	USB Power signal from USB VBUS. Default: internal pull-low (Schmitt-trigger)
P1[7:0]	B	37~44	29~36	General Purpose I/O pins: P3_1: Access LED P1_4: Device Power Control P1_5: USB Speed LED Indicator (HS/SS) P1_6: Write Protect Function P1_7: One Button Backup Control Default: internal pull-high (Schmitt-trigger), typical current 8mA in output mode.
P3[3:0]	B	45~48	37~40	General Purpose I/O pins Default: internal pull-high (Schmitt-trigger), typical current 8mA in output mode.
VCCK	P	15,34	9,27	1.2V core Power pins
GND	P	1,49	5	Digital ground pins
NC		3,5,6,7,8,9, 10,11,12,14, 33,35, 62	3,4,10,26	No Connection

4.0 External Configuration ROM

4.1 External Configuration ROM

The PL2771 uses external serial memory (EEPROM or Flash) to store the Vendor ID, Product ID, Device Release Number (in device descriptor), Attributes and Max Power setting (in configuration descriptor), String Descriptor and some chip operation mode configuration. The external firmware of PL2771 is also stored in this memory and the maximum size is 28KB. After reset, the firmware in the external memory will be loaded into internal program SRAM.

Two types of serial interface are supported, the one is SPI (Serial Peripheral Interface) and the other is I2C compatible interface. Both interfaces support master mode only. The PL2771 allows the following possible configurations:

- **I2C Serial EEPROM:** This option uses I2C serial EEPROM to store chip configuration data and firmware. Firmware is stored in the EEPROM and will be loaded during system startup.

- **SPI Serial Flash:** This is the recommended option. It behaves the same as the I2C serial memory with this chip but the transfer speed of SPI interface is faster than I2C interface. The SPI interface is a four-pin interface but this chip uses only three pins to communicate with. So the DI and DO are shorted; or better short by a serial 240-ohm resistor.

4.2 Data Structure of External Serial Memory Content

The Configuration ROM is organized as follows:

Table 4-1 EEPROM Address and Content

Address	Content	Note
1:0	Check Word – 0x067B (predefined constant)	
3:2	Vendor ID (idVendor field of Device Descriptor)	
5:4	Product ID (idProduct field of Device Descriptor)	
7:6	Device Release Number (bdcDevice field of Device Descriptor)	
8	Attributes (bmAttributes field of Configuration Descriptor)	
9	Max Power (MaxPower field of Configuration Descriptor)	
10	Chip operation settings	
15:14	Reserved	
249:16	USB String Descriptor Table	
253:250	GPIO Settings	
255:254	Miscellaneous	

From byte 16 to byte 230 are used for USB string descriptors. The String Descriptor table is a linked data structure that holds all string descriptors recognized by this chip in the order of its index. The first entry, String 0, represents the Language ID, as defined by the USB specification. The second entry, String 1, is the Manufacturer Descriptor, as defined by the Device Descriptor. The third and forth entries, String 2 and 3, are the Product Descriptor and Serial Number, respectively, also defined by the Device Descriptor. The user has the option to define String 4, 5, and 6 for their own private use. Each of these String Descriptor Entries is of the following data structure:

Table 4-2 String Descriptor Data Structure

Offset	Field	Size	Value	Note
0	bLength	1	Length of the string plus 2, i.e. (N + 2).	
1	bDescriptorType	1	03h – STRING Descriptor type.	
2	bString	N	UNICODE encoded string.	

The last entry of this table must have a bLength of 0 to indicate the end of this table. A zero-length data will be returned if the host tries to access to the string descriptor beyond the last one.

The following table shows one example of valid EEPROM contents:

Table 4-3 Example of Valid EEPROM Contents

Offset	Content	Note
0:1	Check Word – 0x067B	Constant
2:3	Vendor ID – 0x067B	
4:5	Product ID – 0x2771	
6:7	Device Release Number – 0x0100	
8		
9		
15:10		
16	0x04	String Index 0 (4 Bytes)
17	0x03	
19:18	0x0409	Language ID for English (United States).
20	0x32	String Index 1 (50 Bytes)
21	0x03	
69:22	‘X’, 0x00, ‘X’, 0x00, ‘X’, 0x00, ‘ ‘, 0x00, ‘T’, 0x00, ‘e’, 0x00, ‘c’, 0x00, ‘h’, 0x00, ‘n’, 0x00, ‘o’, 0x00, ‘l’, 0x00, ‘o’, 0x00, ‘g’, 0x00, ‘y’, 0x00, ‘ ‘, 0x00, ‘I’, 0x00, ‘n’, 0x00, ‘c’, 0x00, ‘.’ , 0x00	“XXX Technology Inc.” – manufacturer description. 0x00 is padded for UNICODE.
70	0x34	String Index 2 (52 Bytes)
71	0x03	

121:72	‘M’, 0x00, ‘a’, 0x00, ‘s’, 0x00, ‘s’, 0x00, ‘ ‘, 0x00, ‘S’, 0x00, ‘t’, 0x00, ‘o’, 0x00, ‘r’, 0x00, ‘a‘, 0x00, ‘g’, 0x00, ‘e’, 0x00, ‘ ’, 0x00, ‘D’, 0x00, ‘e’, 0x00, ‘v’, 0x00, ‘i’, 0x00, ‘c’, 0x00, ‘e’, 0x00	“Mass Storage Device” – device description. 0x00 is padded for UNICODE.
122	0x0A	String Index 3 (10 bytes)
123	0x03	
131:124	‘0’, 0x00, ‘1’, 0x00, ‘2’, 0x00, ‘3’, 0x00	“3210” – serial number,
132	0x00	End of String Descriptor Table.

The user could also define other strings, 4 to 6, to hold useful information for the drivers and/or applications, such as software authorization codes, symbolic names, just to name a few. However, the total length of this table must not exceed 256 bytes (include reserved space for chip controlling), the supported maximum size of external configuration ROM.

5.0 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5-1 Absolute Maximum Ratings

SYMBOL	DESCRIPTION	RATING	UNIT
VCCK	Core Power Supply	-0.5 ~ 1.6	V
VCC3IO	Power Supply of 3.3 V I/O Cells	-0.5 ~ 3.6	V
V_{IN3}	Input Voltage of 3.3V I/O Cells	-0.5 ~ 3.6	V
T_{STG}	Storage Temperature	-65 ~ 150	^{o}C
I_{IN}	DC Input Current	50	mA
I_{OUT}	Output Short Circuit Current	50	mA

Notes:
1. Permanent damage on devices may occur if the absolute maximum ratings are exceeded. These are only stress ratings, and functional operation should be restricted within the conditions detailed in this table. Exposure to the absolute maximum rating conditions for extended periods of time may affect the reliability of the devices.
2. The input and output negative voltage rating may be exceeded if the input and output currents under ratings are observed.

5.2 Recommended Operating Conditions

Table 5-2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VCCK	Core Power Supply	1.14	1.2	1.26	V
VCC3IO	Power Supply of 3.3V	2.97	3.3	3.63	V
T_j	Junction Operating Temperature	-40	25	125	^{o}C

5.3 DC Characteristics of 3.3V Programmable I/O Cells

Table 5-3 DC Characteristics of 3.3V Programmable I/O Cells

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage	3.3 V LVTTL	-	-	0.8	V
V_{IH}	Input High Voltage		2.0	-	-	V
V_{t-}	Schmitt-trigger negative to threshold voltage	3.3V LVTTL	0.8	1.1	-	V
V_{t+}	Schmitt-trigger positive to threshold voltage		-	1.6	2.0	V
V_{ol}	Output low voltage	$\|I_{ol}\|$ = 2mA~16mA	-	-	0.4	V
V_{oh}	Output high voltage	$\|I_{oh}\|$ = 2mA~16mA	2.4	-	-	V
R_{pu}	Input pull-up resistance	PU = High PD = Low	40	75	190	kΩ
R_{pd}	Input pull-down resistance	PU = Low PD = High	40	75	190	kΩ

5.4 Power On Sequence and Reset Timing

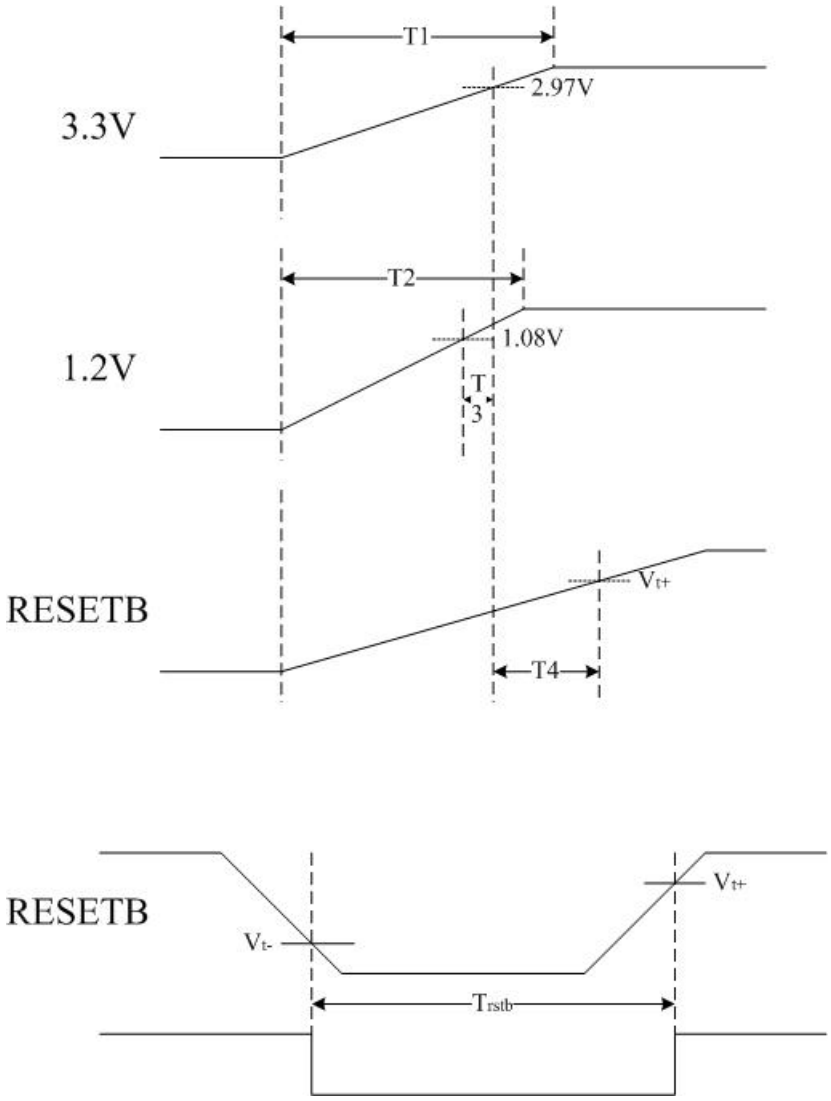


Figure 5-1 Power On Sequence and Reset Timing Diagram

Table 5-4 Recommended Timing

SYMBOL	MIN	TYP	MAX	UNIT
T1	-	-	1	ms
T2	-	-	1	ms
T3	0	>=0	-	ms
T4	2	-	-	ms
T_{rstb}	2	4	-	ms

Note: For Vt+ and Vt-, refer to Table 5-3.

5.5 Operating Current Parameters

Table 5-5 Operating Current Parameters

SYMBOL	PARAMETER	USB Mode	VCC33	VCC12	UNIT
I_{DD}	Operating Current	USB 3.0	40	248	mA
		USB 2.0	24	132	mA
I_{SUS}	Suspend Current (S1 Sleep, Self-Powered)	USB 3.0	3	128	mA
		USB 2.0	6	125	mA
	Suspend Current (S4 Hibernate, Self-Powered)	USB 3.0	3	128	mA
		USB 2.0	6	113	mA

Test Environment Machine: Gigabyte GA-P55A-UD4P Motherboard with on-board NEC USB 3.0 chip.

5.6 Crystal/Oscillator Frequency

The recommended crystal or oscillator frequency is 30MHz ± 50ppm.

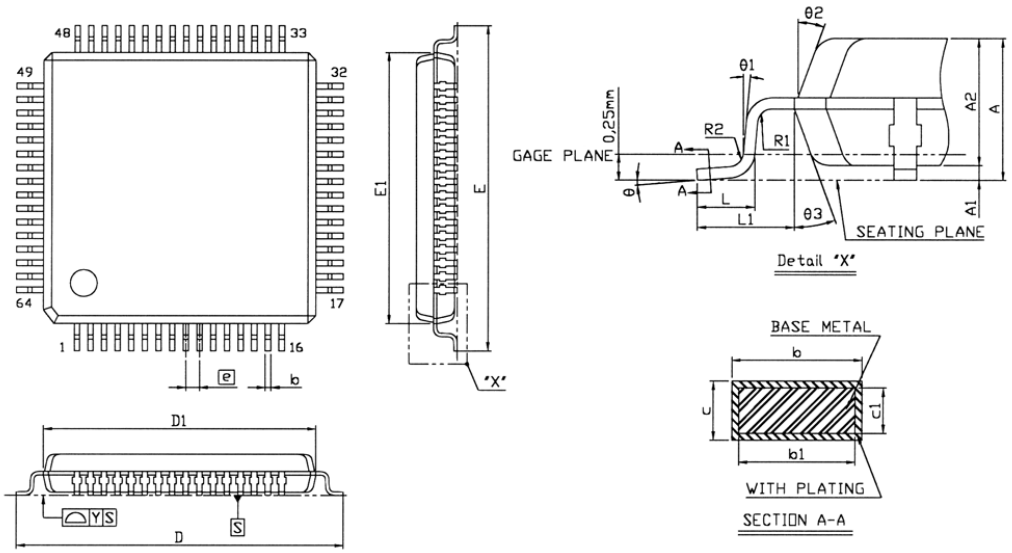
6.0 Ordering Information

Table 6-1 Ordering Information

Part Number	Package Type
PL2771 LQFP64	64-pin LQFP (10x10mm)
PL2771 QFN48	48-pin QFN (7x7mm)

7.0 Outline Diagram

7.1 LQFP64 Package (10x10mm) Outline Diagram

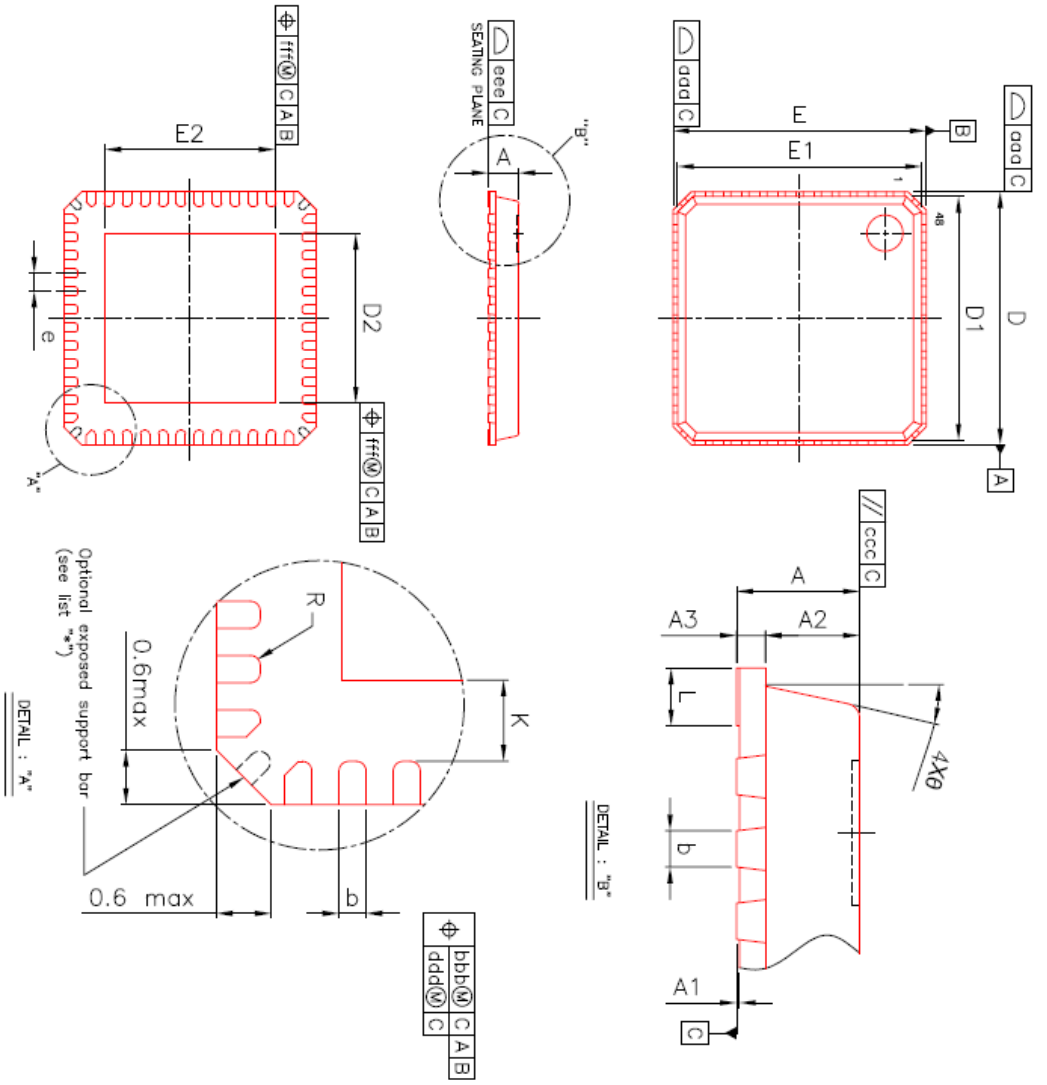


SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1,60			63
A1	0,05		0,15	2		6
A2	1,35	1,40	1,45	53	55	57
b	0,17	0,22	0,27	7	9	11
b1	0,17	0,20	0,23	7	8	12
c	0,09		0,20	4		8
c1	0,09		0,16	4		6
D	12,00 BSC			472 BSC		
D1	10,00 BSC			394 BSC		
E	12,00 BSC			472 BSC		
E1	10,00 BSC			394 BSC		
e	0,50 BSC			20 BSC		
L	0,45	0,60	0,75	18	24	30
L1	1,00 REF			39 REF		
R1	0,08			3		
R2	0,08		0,20	3		8
Y			0,075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

NOTES:
1.REFER TO JEDEC MS-026/BCD
2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE
MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE
DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED
THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4.ALL DIMENSIONS IN MILLIMETERS.

Figure 7-1 Outline Diagram of PL2771 LQFP64 (10x10mm)

7.2 QFN48 Package (7x7mm) Outline Diagram



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.70	0.024	0.026	0.028
A3		0.20 REF			0.008 REF	
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E		7.00 BSC			0.276 BSC	
D1/E1		6.75 BSC			0.266 BSC	
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	----	14°	0°	----	14°
R	0.09	----	----	0.004	----	----
K	0.20	----	----	0.008	----	----
aaa	----	----	0.15	----	----	0.006
bbb	----	----	0.10	----	----	0.004
ccc	----	----	0.10	----	----	0.004
ddd	----	----	0.05	----	----	0.002
eee	----	----	0.08	----	----	0.003
fff	----	----	0.10	----	----	0.004

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER

	L/F	D2/E2 (mm)			D2/E2 (inch)			*
		MIN	NOM	MAX	MIN	NOM	MAX	
①		4.90	5.05	5.20	0.193	0.199	0.205	NO
②		4.95	5.10	5.25	0.195	0.201	0.207	YES / NO
③		5.31	5.46	5.61	0.209	0.215	0.221	NO
④		3.56	3.71	3.86	0.140	0.146	0.152	NO
⑤		2.95	3.10	3.25	0.116	0.122	0.128	NO

Exposed Pad Size

Figure 7-2 Outline Diagram of PL2771 QFN48 (7x7mm)