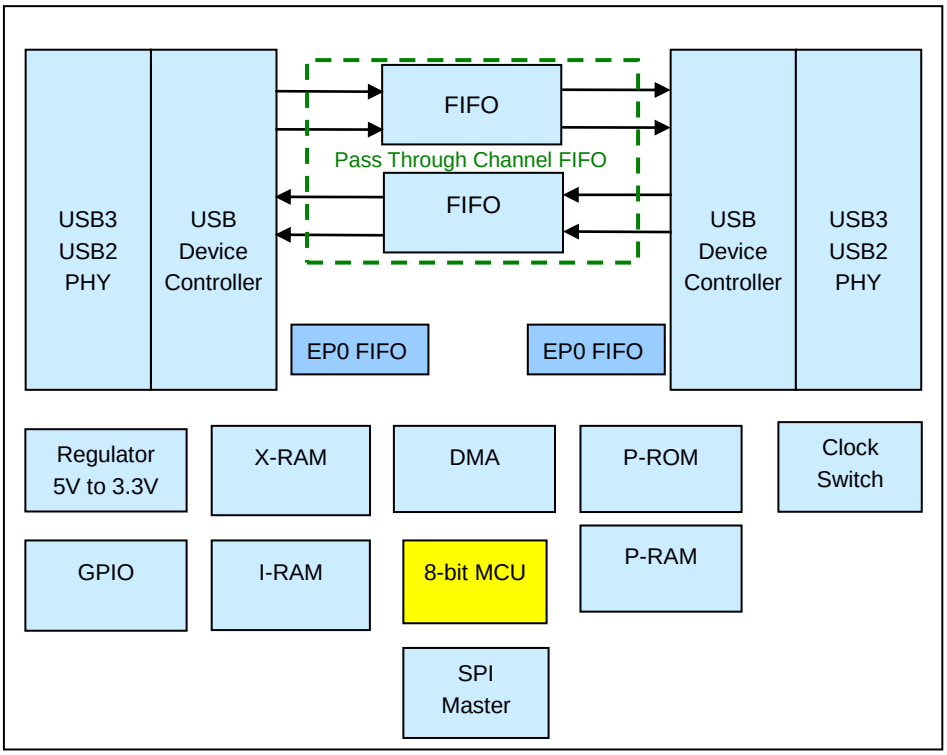
Product Data Sheet PL27A1

- SuperSpeed USB 3.0 Host-to-Host Bridge Controller
- USB 3.0 and USB 2.0 specification compliant
- Transfer data between two PCs via USB port
- Built-in driver (USB Easy Transfer Cable) and software (Windows Easy Transfer) in Windows Vista, Windows 7, and Windows 8. Also supports Windows XP by driver install.
- Application programs can be stored in external SPI Flash by Mass Storage mode
- 8-bit High Performance 1T 8032 MCU
- USB Device Interface
  - 2 x USB Device PHYs
  - Supports 5GHz SuperSpeed, 480MHz Hi-Speed, and 12MHz Full-Speed mode
  - One General Purpose SPI Master controller
  - USB Endpoint 0 for Control Endpoint with dedicated 512 bytes buffer for each USB
  - Highly configurable endpoint structure
  - Pass Through Channel FIFO architecture can utilize full USB bandwidth for data transferring
  - Provides 2 x LED pins
- 3.3V Digital I/O Pad
- 1.2V Power Supply for Core
- Built-in 5V to 3V linear low-dropout regulator
- Embedded Power on Reset (POR)
- 30MHz crystal oscillator for both USB PHYs
- Supports external SPI Flash to customize USB vendor/product ID
- QFN64 Package



System Block Diagram

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Ordering Information

Product	Package Type	Ordering Number
PL27A1	64-pin QFN (9x9mm)	PL27A1A3FKG7P1

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1. Overview

The PL27A1 is a single-chip SuperSpeed USB 3.0 Host-to-Host bridge controller specially designed for Windows USB Easy Transfer cable and Microsoft Windows Easy Transfer (WET) program. SuperSpeed USB has data transfer bandwidth of up to 5Gbps offering 10X performance increase over Hi-Speed USB 2.0 (480Mbps). SuperSpeed USB is backward compatible and interoperates with all USB3.0/USB2.0/USB1.1 hosts, devices, and hubs. The PL27A1 is fully supported by Microsoft for Windows XP, Windows Vista, Windows 7, and Windows 8 OS.

Figure 1-1 Target Application (USB 3.0 Windows Easy Transfer Cable)

Microsoft Windows Easy Transfer (WET) driver and program are built inside Windows Vista, Windows 7, and Windows 8 and also available for installation in Windows XP. Using the Windows Easy Transfer program, the PL27A1 USB 3.0 transfer cable allows end-users to easily connect thru the USB port an old computer running Microsoft Windows XP/Vista/7/8 to another new computer running Windows Vista/7/8. Once the program has established connection for both computers, the end-user can then easily transfer large data files and program settings from the old computer to the new computer. It's the fastest and easiest way to transfer files and program settings from an old Windows PC to a new Windows PC.

The PL27A1 also works with Prolific PCLinq file transfer software. PCLinq is a versatile user-friendly file manager program that allows the end-user to see and control file directories on both PCs at the same time. End-users can easily drag-and-drop or cut-and-paste files and folders between remote and local PCs as well as creating new folders and changing file attributes. PCLinq is designed to be used in addition to Windows Easy Transfer for Windows XP, Vista, 7, and 8.

The PL27A1 also supports read-only BOT (Bulk-only transfer) device using USB mass storage mode and Windows built-in drivers that allows application programs like PCLinq to be stored into the external SPI flash memory.

The PL27A1 chip solution is especially suitable for those who need bulk data transfer between two PCs - either notebook PC or desktop PC.

1.1 Features

- SuperSpeed USB 3.0 Host-to-Host Bridge Controller
- USB 3.0 and USB 2.0 specification compliant
  - SuperSpeed (5Gbps), Hi-Speed (480Mbps), and Full-Speed (12Mbps)
- Transfer data between two PCs via USB port (up to SuperSpeed USB 3.0)
- Built-in driver (USB Easy Transfer Cable) and software (Windows Easy Transfer) in Windows Vista, Windows 7, and Windows 8. Windows XP driver and software can be downloaded from Microsoft or bundled with end-product CD.
- Prolific can provide royalty-free PCLinq software for Windows XP/Vista/7/8/8.1 for easy file management between two PCs.
- Application programs can be stored in external SPI Flash. This SPI Flash is enumerated by USB Mass Storage and will appear as a read-only disk drive.
- 8-bit high-performance 1T 8032 MCU
- USB device interface
  - Two USB device PHYs
  - USB endpoint 0 for control endpoint with dedicated 512 bytes buffer for each USB side
  - Highly configurable endpoint structure. Each endpoint can be configured as interrupt, bulk, and isochronous endpoint.
  - Pass Through Channel FIFO architecture can utilize full USB bandwidth for data transferring
- Peripherals
  - One SPI Flash Controller for external SPI Serial Flash Memory
    - Supports DMA feature between external SPI flash and internal FIFO
    - Supports multi-vendor SPI Serial Flash Memory
- 3.3V Digital I/O Pad
- 1.2V power supply for core
- Built-in 5V to 3V linear low-dropout regulator
- Embedded power-on reset (POR)
- 30MHz crystal oscillator (shared by both USB PHYs)
- Supports external SPI Flash to customize USB vendor/product ID
- Supports LED indicator for connection and transfer status
- Bus powered from either USB port
- QFN64 Package

2. Functional Block Diagram

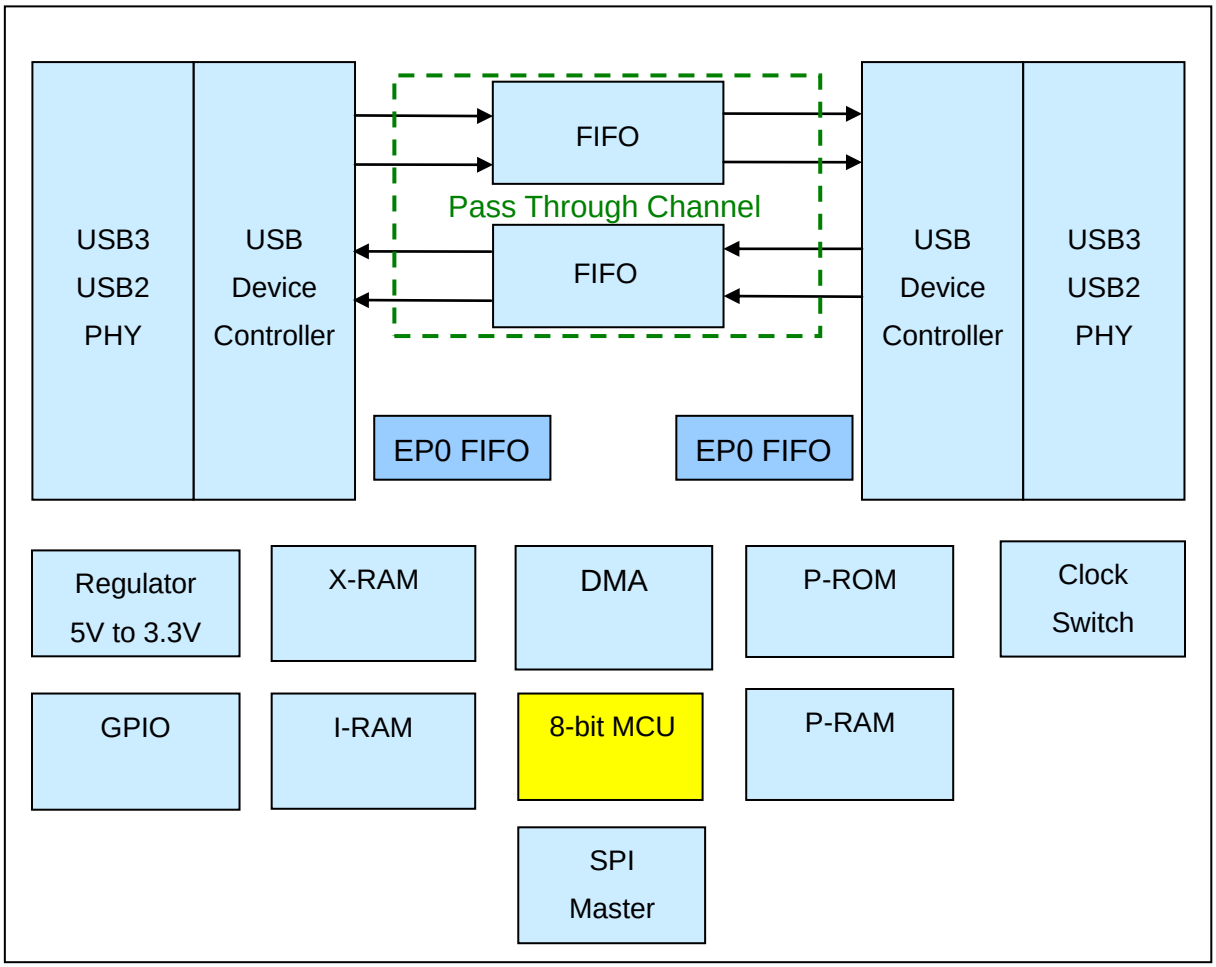


Figure 2-1 Functional Block Diagram

3. Pin Diagram

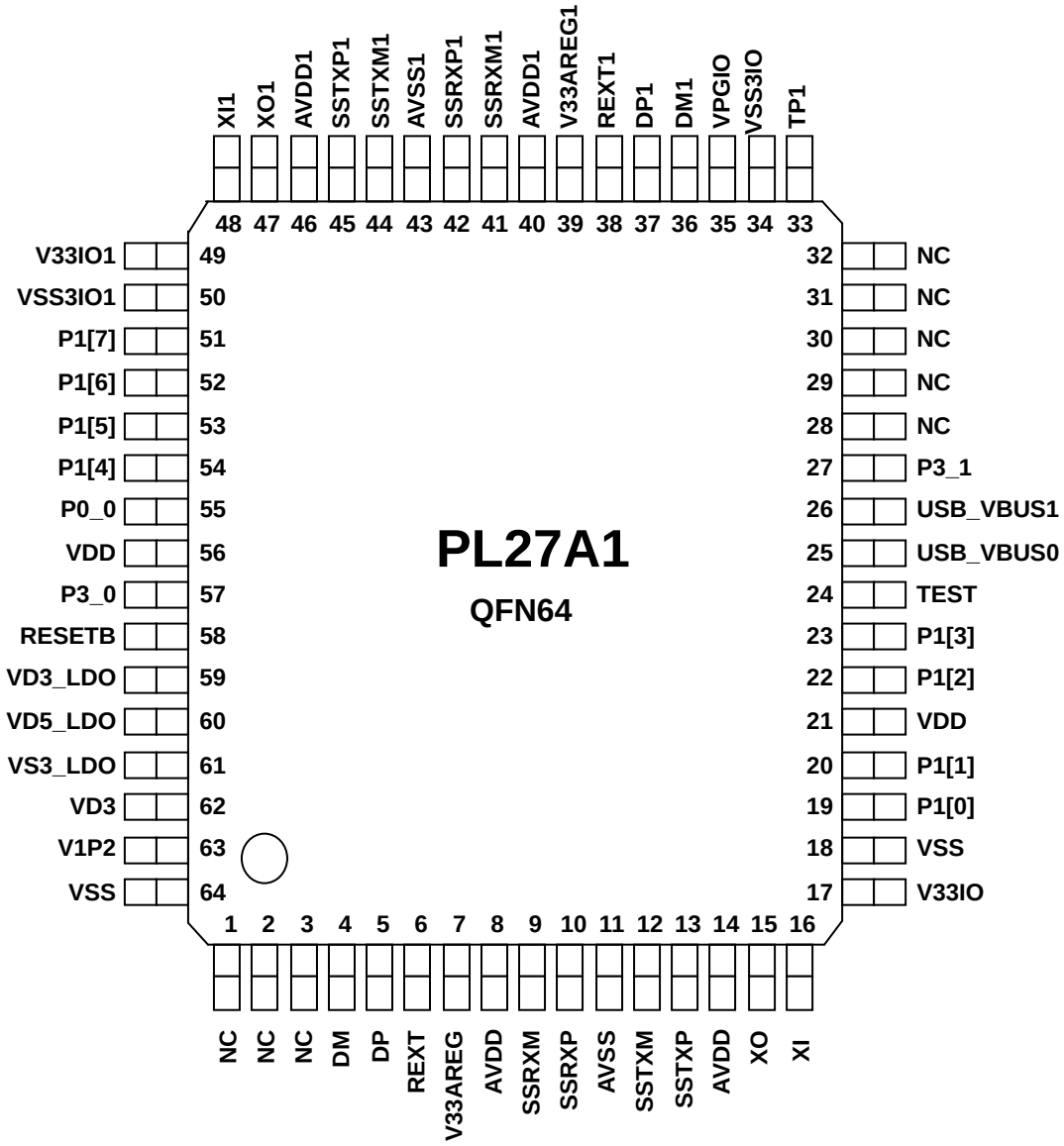


Figure 3-1 PL27A1 Pin Diagram (QFN64)

4. Pin Assignment & Description

Pin Type Abbreviation:

I: Input	O: Output	B: Bidirectional	A: Analog	P: Power/Ground

4.1 USB0 PHY Related Pins

Table 4-1 USB0 PHY Related Pins

Symbol	Type	Pin No	Description
DP	B	4	High speed D+ signal
DM	B	5	High speed D- signal
REXT	A	6	Connect external resistor to analog ground
V33AREG	P	7	Analog power 3.3V for on-chip USB 2.0 PHY
AVDD	P	8	Analog power 1.2V for on-chip USB PHY
SSRXM	I	9	SuperSpeed RXM signal
SSRXP	I	10	SuperSpeed RXP signal
AVSS	P	11	Analog power 3.3V for on-chip USB PHY
SSTXM	O	12	SuperSpeed TXM signal
SSTXP	O	13	SuperSpeed TXP signal
AVDD	P	14	Analog power 1.2V for on-chip USB PHY
XO	B	15	Crystal oscillator 30MHz clock output
XI	I	16	Crystal oscillator 30MHz clock input
AVDD3/V33IO	P	17	Analog power 3.3V for on-chip USB PHY

4.2 USB1 PHY Related Pins

Table 4-2 USB1 PHY Related Pins

Symbol	Type	Pin No	Description
DP1	B	36	High speed D+ signal
DM1	B	37	High speed D- signal
REXT1	A	38	Connect external resistor to analog ground
V33AREG1	P	39	Analog power 3.3V for on-chip USB 2.0 PHY
AVDD1	A	40	Analog power 1.2V for on-chip USB PHY
SSRXM1	I	41	SuperSpeed RXM signal
SSRXP1	I	42	SuperSpeed RXP signal
AVSS1	P	43	Analog power 3.3V for on-chip USB PHY
SSTXM1	O	44	SuperSpeed TXM signal
SSTXP1	O	45	SuperSpeed TXP signal
AVDD1	P	46	Analog power 1.2V for on-chip USB PHY
XO1	B	47	Crystal oscillator 30MHz clock output
XI1	I	48	Crystal oscillator 30MHz clock input
AVDD31/V33IO1	P	49	Analog power 3.3V for on-chip USB PHY

4.3 System Pins

Table 4-3 System Pins

Symbol	Type	Pin No	Description
VSS3IO	P	18	3.3V I/O ground
P1[0]	B	19	LED_TRAN: P1[0] – Control pin for LED behavior during data transfer operation of relative USB side.
P1[1]	B	20	LED_TRAN: P1[1] – Control pin for LED behavior during data transfer operation of relative USB side.
VDD	P	21	1.2V core power
P1[2]	B	22	GPIO P1[2]
P1[3]	B	23	GPIO P1[3]
TEST	I	24	Chip Test mode enable. Must be NC or tied to Ground.
USB_VBUS0	I	25	USB power signal from side 0 USB VBUS
USB_VBUS1	I	26	USB power signal from side 1 USB VBUS
P3_1	B	27	LED_indicator: Control pin for single LED mode during any side data transfer operation.
TP1	I	33	Must be pulled down(4.7KΩ) to GND.
VSS3IO	P	34	3.3V I/O ground
VPGIO	P	35	3.3V Power pin
VSS3IO1	P	50	3.3V I/O ground
P1[7]	B	51	Must be floating if not used.
P1[6]	B	52	Must be floating if not used.
P1[5]	B	53	Serial Flash Data Output. Must be floating if not used.
P1[4]	B	54	Serial Flash Data Input. Must be floating if not used.
P0[0]	B	55	Serial Flash Clock Input. Must be floating if not used.
VDD	P	56	1.2V Core Power
P3_0	B	57	Serial Flash Chip Select. Must be floating if not used.
RESETB	I	58	External reset pin, active low
VD3_LDO	P	59	3.3V LDO regulator output voltage
VD5_LDO	P	60	5V LDO regulator input voltage
VS3_LDO	P	61	Ground of LDO
VD3	P	62	3.3V regulator input voltage (from LDO output)
V1P2	P	63	1.2V Power Input
VSS	P	64	Ground
NC	B	1,2,3, 28~32	No Connection. Keep floating.

5. Functional Description

5.1 USB3 / USB2 PHY

The USB physical layer IP generates and responds USB electrical signals. These two USB physical layers IP comply with USB 3.0 and USB 2.0 specification. The USB 3.0 part uses PIPE interface to communicate with USB 3.0 controller while the USB 2.0 part uses UTMI interface to communicate with USB 2.0 controller.

5.2 USB Device Controller

The USB device controller generates and decodes USB transactions including packet header, CRC check, data payload, etc. This controller acts as USB device that can accept host transaction and responds data or status. Each USB device controller has dedicated control endpoint FIFO to handle USB SETUP token and its data transfer.

5.3 Pass-Through Channel FIFO

The Pass-Through Channel FIFO can be used to transfer data packet between two USB controllers side. When the data packet is inputted from one USB side, the other side can output it directly. There are two pairs (IN and OUT) pass-through channels in this chip.

5.4 EP0 FIFO

The EP0 FIFO is used to endpoint 0 transfer data packet only for each side and the size is a maximum packet size of every USB speed mode.

5.5 Regulator

The Regulator IP is included to generate IO 3.3V supply voltage.

5.6 Clock Switch

Clock switch is designed to handle clock switch between two sides USB at attach/detach and suspend/resume state.

5.7 8-bit MCU

This chip uses high performance 1T 8032 8-bit microcontroller. It provides higher performance than general 8032 MCU.

5.8 P-ROM

There is a Program ROM in this chip. After power on reset, the MCU of this chip runs program from this Program ROM (P-ROM).

5.9 256B I-RAM

256 bytes IDATA RAM for 8032 MCU. This memory space can provide high speed scratchpad memory for MCU.

5.10 X-RAM

XDATA RAM for 8032 MCU. This is MCU data memory located at XDATA space and MCU uses it to store data in process.

5.11 GPIO and PWM

Two PWM signal generators which can be used to control LED flashing behavior. There are also some GPIO signals that can be controlled directly by MCU. These signals are multiplexed with peripherals. If some peripherals are turned on, the GPIO signals which is multiplexed will be disabled and these signals change to peripheral signals.

5.12 DMA

The DMA controller is used to transfer data between FIFO XDATA RAM and peripherals. MCU can control this DMA to get data from FIFO or to put data to FIFO from XDATA RAM. It can also be used to transfer data between P-RAM to SPI flash controller or eMMC flash controller.

5.13 SPI Flash Controller

SPI Flash Controller can be used to access data of SPI serial flash memory. The SPI clock rate can be adjusted by MCU.

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 6-1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{CCK}	1.2V Core Power Supply	-0.3 to 1.4	V
V_{CC}	3.3V Power Supply	-0.3 to 4.0	V
V_{D5}	5V Power Supply	-0.3 to 6.0	V
V_{IN3}	Input Voltage of 3.3V I/O	-0.3 to V_{CC3I} +0.3	V
	Input Voltage of 3.3V I/O with 5V Tolerance	-0.3 to 5.5	
T_{STG}	Storage Temperature	-40 to 150	^{o}C

6.2 Recommended Operating Conditions

Table 6-2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{D5}	5V Power Supply	4.5	5	5.5	V
V_{CCK}	1.2V Core Power Supply	1.14	1.2	1.26	V
V_{CC3I}	Power Supply of 3.3V I/O	3.0	3.3	3.6	V
T	Operating Temperature	0	25	70	^{o}C

6.3 Recommended Operating Conditions of 3.3V GPIO

Table 6-3 Recommended Operating Conditions of 3.3V GPIO

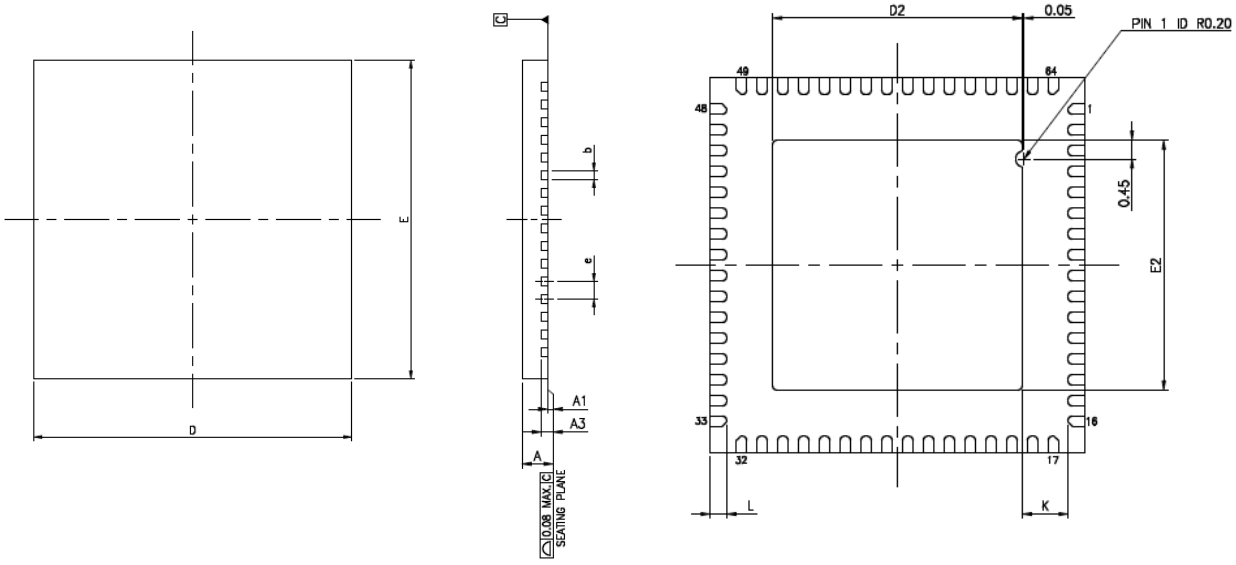
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{DD33}	I/O Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0		5.5	V
V_{IL}	Input Low Voltage	-0.3		0.8	V
R_{PU}	Pull-up Resistor	62	77	112	kΩ
V_{OL}	Output Low Voltage			0.4	V
V_{OH}	Output High Voltage	2.4			V
I_{OL}	Low Level Output Current @V_{OL} =0.4V	8			mA
I_{OH}	High Level Output Current @V_{OL} =2.4V	12			mA

6.4 Operating Current

Table 6-4 Operating Current

Symbol	Parameter	Connection	Current of 3.3V	Current of 1.2V	Units
I_{DD}	Operating Current	USB 3.0	57	251	mA
		USB 2.0	41	85	mA
I_{SUS}	Suspend Current (Sleep, bus-powered)	USB 3.0	0.6	0.8	mA
		USB 2.0	0.9	0.65	mA

7. Outline Diagram



	PACKAGE TYPE		
JEDEC OUTLINE	MO-220		
PKG CODE	VQFN (Y964)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
B	0.18	0.25	0.30
D	9.00 BSC		
E	9.00 BSC		
e	0.50 BSC		
K	0.20	-	-

	E2			D2			L			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
244x244 MIL	5.90	6.00	6.05	5.90	6.00	6.05	0.35	0.40	0.45	V	X	(V) WMMD-4

NOTES:

1. All dimensions are in millimeters.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

Figure 7-1 Outline Diagram of QFN64

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