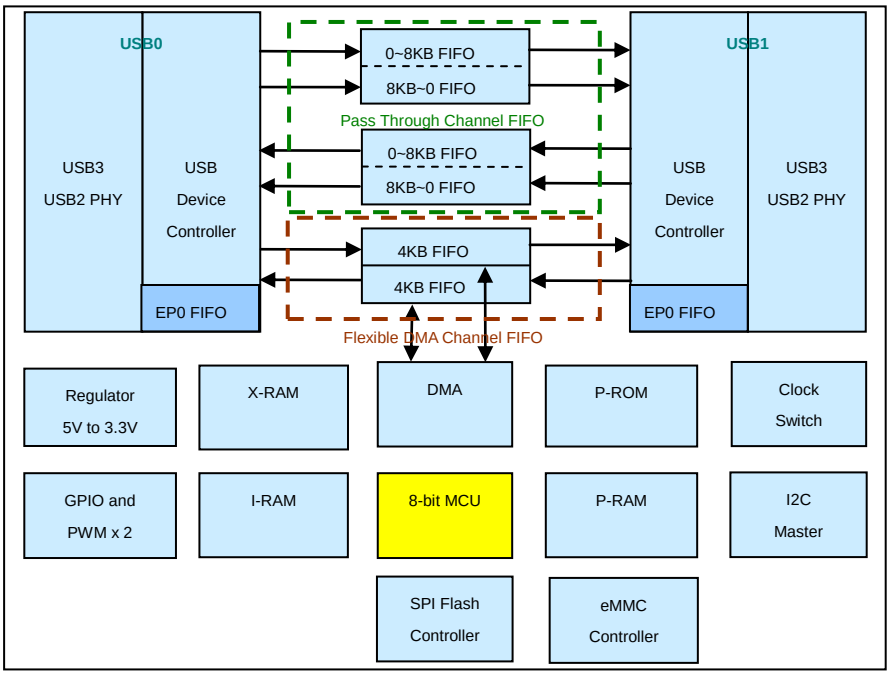
Product Data Sheet PL2701

- High Performance USB 3.0 Host to Host Bridge Controller
- USB 3.0 and USB 2.0 Specification Compliant
- 8-bit High Performance 1T 8032 MCU
  - MCU clock rate can be 30MHz or 60MHz
  - Support watchdog timer
- USB Device Interface
  - Two USB Device PHYs
  - Supports 5Gbps SuperSpeed, 480Mbps Hi-Speed, and 12Mbps Full-Speed mode
  - USB Endpoint 0 for Control Endpoint with dedicated 512 bytes buffer for each USB
  - Support 16 endpoints
  - Hybrid FIFO channels (Pass Through FIFO Channel and Flexible DMA FIFO Channel) for versatile performance and flexibility applications
- Peripherals
  - One General Purpose single byte buffer I2C master controller with data rate up to 1Mbps
  - One SPI Flash Controller for external SPI Serial Flash memory
  - One eMMC Reader Interface for external eMMC flash memory
  - 2 PWM Controllers support frequency 1Hz to 20KHz with 8 bit duty cycle control
  - UART Interface with TXD/RXD from 8032 MCU
  - Provides up to 16 General Purpose I/O pins
- 3.3V Digital I/O Pad
- 1.2V Power Supply for Core
- Built-in 5V to 3V linear low-dropout regulator
- Embedded Power on Reset (POR)
- 30MHz crystal for USB PHY
- QFN64 Package



System Block Diagram

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Ordering Information

Product	Package Type	Ordering Number
PL2701	64-pin QFN (9x9mm)	PL2701A3FKG7P1

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1. Overview

The PL2701 is a single-chip SuperSpeed USB 3.0 Host-to-Host bridge controller specially designed for connecting two USB Host devices either between Desktop/Laptop PC, Tablet, SmartPhone, or Smart TV with Windows, Mac, iOS, or Android OS installed. SuperSpeed USB 3.0 has data transfer bandwidth of up to 5Gbps offering 10X faster performance over Hi-Speed USB 2.0 (480Mbps) and is backward compatible with all USB3.0/USB2.0/USB1.1 hosts, devices, and hubs.

The PL2701 uses “Hybrid Multi-Class” channel that allows two USB host devices to share keyboard/mouse, network, mass storage, display, and multimedia capabilities. The PL2701 links two USB hosts to exchange data through RNDIS (Remote Network Driver Interface Specification) and supports HID (Human Interface Device) interface including keyboard/mouse. Both USB sides support mass storage mode to read external flash memory. The PL2701 also provides flexible endpoint assignment mechanism to easily support multi-USB class protocol. Many applications can be implemented through this high performance controller.

Prolific provides the ULinQ App software that allows end-users not only to share files but also to control or use the display, storage, and multimedia capabilities of the other host device. The ULinQ feature creates a brand new user-experience in sharing mobile contents and apps to other smart devices with larger display.

1.1 Product Concept and Application

Figure 1-1 Product Concept and Application

1.2 Features

- MCU
  - 8-bit high performance 1T 8032 MCU
  - 8032 clock generated from USB PHY
  - MCU clock rate can be 30MHz or 60MHz
- USB Device Interface
  - Two USB device PHYs
  - USB implementation is compliant with USB 2.0 and USB 3.0 specification
  - Supports 5Gbps super speed, 480MHz high speed and 12MHz full speed
  - USB endpoint 0 for control endpoint with dedicate 512 bytes buffer for each side USB
  - Supports 16 endpoints (excluding endpoint 0)
    - configurable as interrupt, bulk, and isochronous endpoints
    - divided to two parts, 8 input and 8 output endpoints
  - Hybrid FIFO channels (Pass Through FIFO Channel and Flexible DMA FIFO Channel) for versatile performance and flexibility applications
  - Pass through FIFO channel
    - Two pair 8KB FIFOs sharing by two endpoints which need high performance transfer
  - Flexible DMA FIFO channel
  - One pair 4KB FIFO sharing by remaining 6 endpoints
  - data transfer between these 4KB FIFOs can be controlled by MCU
- Peripherals
  - One general purpose single byte buffer I2C master controller with data rate up to 1Mbps
  - One SPI flash controller which control external SPI serial Flash memory
    - Supports DMA feature between external SPI flash and USB flexible DMA FIFO
    - Supports DMA feature between external SPI flash and internal Program RAM
    - SPI frequency up to 60MHz
  - One eMMC reader interface which control external eMMC flash memory
    - Supports DMA feature between external eMMC flash and USB flexible DMA FIFO
    - Supports DMA feature between external eMMC flash and internal Program RAM
    - Supports 4 data bits interface
    - eMMC frequency up to 30MHz
  - 2 PWM controllers support frequency 1Hz to 20KHz with 8 bit duty cycle control
  - UART interface with TXD/RXD comes from 8032 MCU
  - Provides up to 16 general purpose I/O pins
    - GPIOs share same package pins with other peripherals
- 3.3V Digital I/O Pad
- 1.2V Power Supply for core
- Built-in 5V to 3V linear low-dropout regulator
- Embedded Power On Reset
- 30MHz crystal for USB PHY
- QFN64 Package (9mmx9mm)

2. Block Diagram

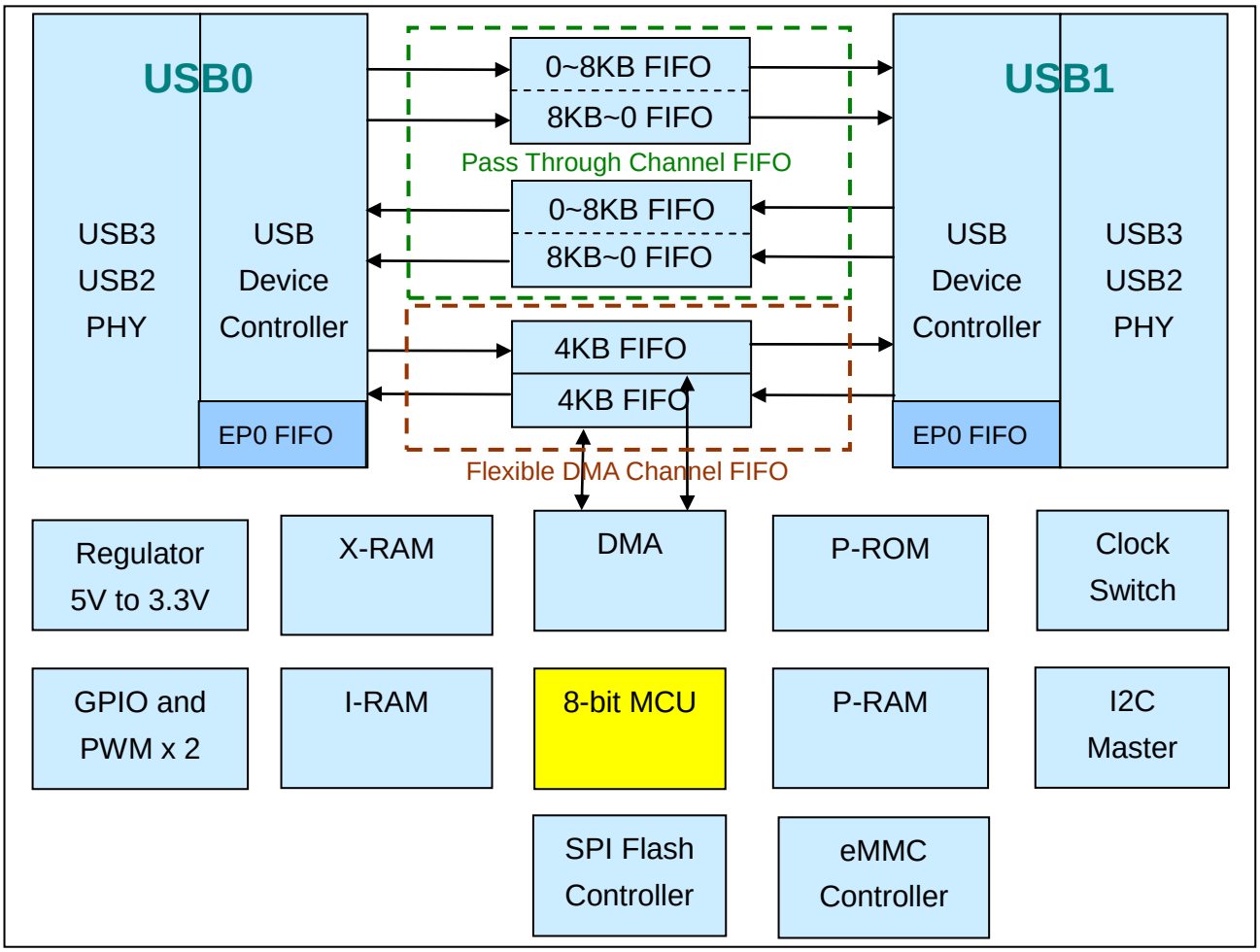


Figure 2-1 System Block Diagram

3. Pin Diagram

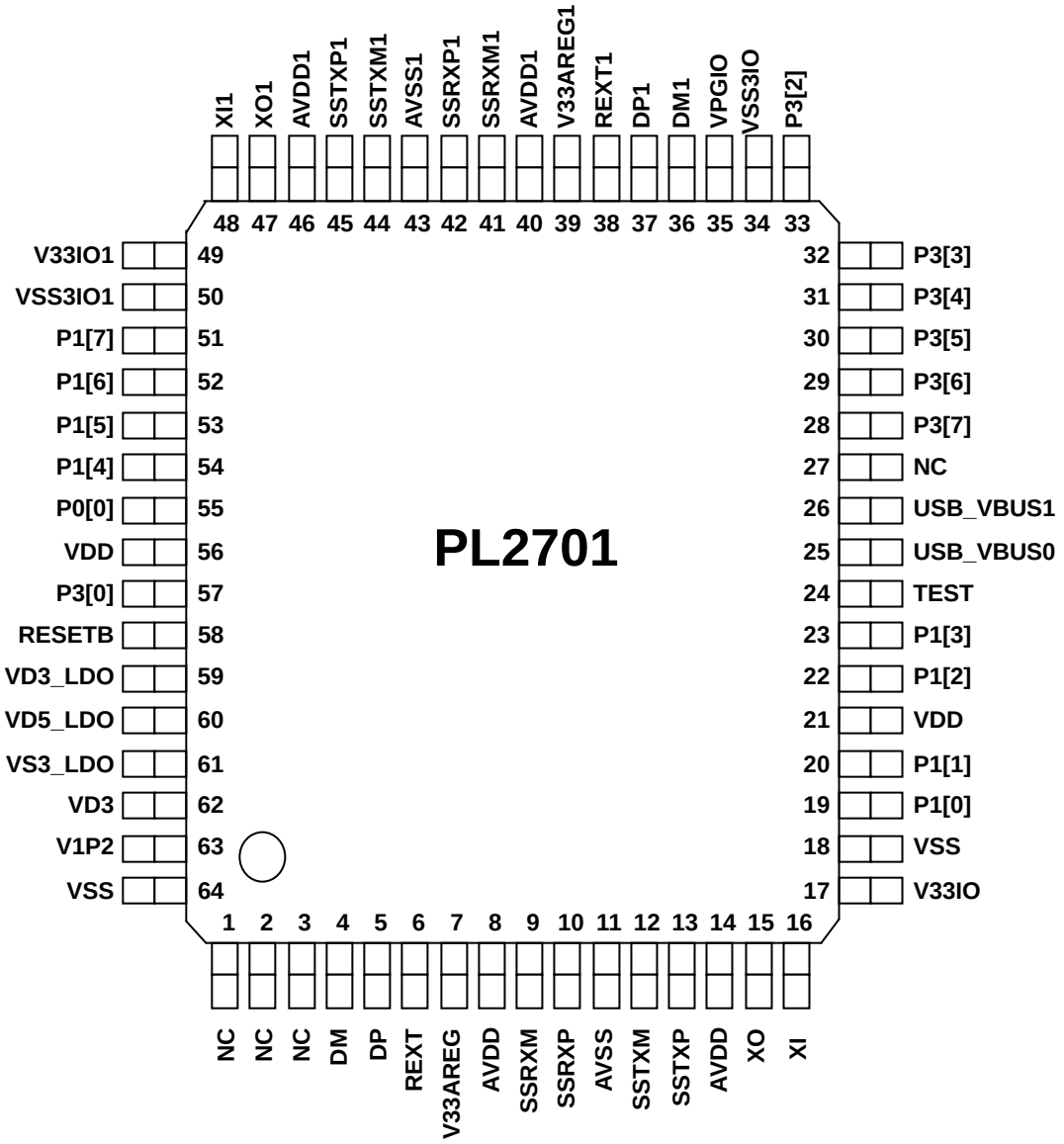


Figure 3-1 PL2701 QFN64 Pin Diagram

4. Pin Assignment & Description

Pin Type Abbreviation:

I: Input	O: Output	B: Bidirectional	A: Analog	P: Power/Ground

4.1 USB0 PHY Related Pins

Table 4-1 USB0 PHY Related Pins

Symbol	Type	Pin No	Description
DM	B	4	High speed D- signal
DP	B	5	High speed D+ signal
REXT	A	6	Connect external resistor to analog ground
V33AREG	P	7	Analog power 3.3V for on-chip USB 2.0 PHY
AVDD	P	8	Analog power 1.2V for on-chip USB PHY
SSRXM	I	9	SuperSpeed RXM signal
SSRXP	I	10	SuperSpeed RXP signal
AVSS	P	11	Analog power 3.3V for on-chip USB PHY
SSTXM	O	12	SuperSpeed TXM signal
SSTXP	O	13	SuperSpeed TXP signal
AVDD	P	14	Analog power 1.2V for on-chip USB PHY
XO	B	15	Crystal oscillator 30MHz clock output
XI	I	16	Crystal oscillator 30MHz clock input
AVDD3 (V33IO)	P	17	Analog power 3.3V for on-chip USB PHY

4.2 USB1 PHY Related Pins

Table 4-2 USB1 PHY Related Pins

Symbol	Type	Pin No	Description
DM1	B	36	High speed D- signal
DP1	B	37	High speed D+ signal
REXT1	A	38	Connect external resistor to analog ground
V33AREG1	P	39	Analog power 3.3V for on-chip USB 2.0 PHY
AVDD1	A	40	Analog power 1.2V for on-chip USB PHY
SSRXM1	I	41	SuperSpeed RXM signal
SSRXP1	I	42	SuperSpeed RXP signal
AVSS1	P	43	Analog power 3.3V for on-chip USB PHY
SSTXM1	O	44	SuperSpeed TXM signal
SSTXP1	O	45	SuperSpeed TXP signal
AVDD1	P	46	Analog power 1.2V for on-chip USB PHY
XO1	B	47	Crystal oscillator 30MHz clock output
XI1	I	48	Crystal oscillator 30MHz clock input
AVDD31 (V33IO1)	P	49	Analog power 3.3V for on-chip USB PHY

4.3 System Pins

Table 4-3 System Pins

Symbol	Type	Pin No	Description
VSS3IO	P	18	3.3V I/O ground
P1[0]	B	19	LED_TRAN: P1[0] – Control pin for LED behavior during data transfer operation.
P1[1]	B	20	LED_TRAN: P1[1] – Control pin for LED behavior during data transfer operation.
VDD	P	21	1.2V core power
P1[2]	B	22	EE_CLK: P1[2]
P1[3]	B	23	EE_DATA: P1[3]
TEST	I	24	Chip Test mode enable. Must be NC or tied to Ground.
USB_VBUS0	I	25	USB power signal from side 0 USB VBUS
USB_VBUS1	I	26	USB power signal from side 1 USB VBUS
P3[7]	B	28	eMMC data lines. Must be floating if not used.
P3[6]	B	29	eMMC data lines. Must be floating if not used.
P3[5]	B	30	eMMC data lines. Must be floating if not used.
P3[4]	B	31	eMMC data lines. Must be floating if not used.
P3[3]	B	32	eMMC Command. Must be floating if not used.
P3[2]	B	33	eMMC Clock Input. Must be tied to GND if not used.
VSS3IO	P	34	3.3V I/O ground
VPGIO	P	35	3.3V Power pin
VSS3IO1	P	50	3.3V I/O ground
P1[7]	B	51	Serial Flash Data I/O. Must be floating if not used.
P1[6]	B	52	Serial Flash Data I/O. Must be floating if not used.
P1[5]	B	53	Serial Flash Data I/O. Must be floating if not used.
P1[4]	B	54	Serial Flash Data I/O. Must be floating if not used.
P0[0]	B	55	Serial Flash Clock Input. Must be floating if not used.
VDD	P	56	1.2V Core Power
P3[0]	B	57	Serial Flash Chip Select. Must be floating if not used.
RESETB	I	58	External reset pin, active low
VD3_LDO	P	59	3.3V LDO regulator output voltage
VD5_LDO	P	60	5V LDO regulator input voltage
VS3_LDO	P	61	Ground of LDO
VD3	P	62	3.3V regulator input voltage (from LDO output)
V1P2	P	63	1.2V Power Input
VSS	P	64	Ground
NC	B	1,2,3,27	No Connection. Keep floating.

5. Functional Description

5.1 USB 3/USB 2 PHY

The USB Physical layer IP generates and responds USB electrical signals. These two USB Physical layer IP comply with USB 3.0 and USB 2.0 specification. The USB 3.0 part uses PIPE interface to communicate with USB 3.0 controller while the USB 2.0 part uses UTMI interface to communicate with USB 2.0 controller.

5.2 USB Device Controller

The USB device controller generates and decodes USB transactions including packet header, CRC check, data payload, etc. This controller acts as USB device that can accept host transaction and responds data or status. Each USB device controller has dedicated control endpoint FIFO to handle USB SETUP token and its data transfer.

5.3 Pass-Through Channel FIFO

The Pass-Through Channel FIFO can be used to transfer data packet between two USB controllers side. When the data packet is inputted from one USB side, the other side can output it directly. Data manipulation by this chip is not possible. There are two pairs (IN and OUT) pass-through channels in this chip.

5.4 Flexible DMA Channel FIFO

The FIFO in Flexible DMA Channel not only can send/receive USB data packet to/from USB device controller. It can also transfer data between FIFO and MCU XDATA RAM through DMA controller. The data flow between USB device controller and FIFO can be turned off (blocked) or turned on by MCU controlling. Both USB device controllers share same pair (IN and OUT) flexible DMA channel FIFO.

5.5 EP0 FIFO

The EP0 FIFO is used to endpoint 0 transfer data packet only for each side and the size is a maximum packet size of every USB speed mode.

5.6 Regulator

The Regulator IP is included to generate core IO 3.3V supply voltage.

5.7 Clock Switch

Because there are two USB sides, either side of the USB may enter attach/detach or suspend/resume state. The FIFO and MCU shall switch chip clock from different USB side.

5.8 8-bit MCU

High performance 1T 8032 8-bit microcontroller. It provides higher performance than general 8032 MCU.

5.9 P-ROM

There is a Program ROM in this chip. After power on reset, the MCU of this chip runs program from this Program ROM (P-ROM).

5.10 X-RAM

XDATA RAM for 8032 MCU. This is MCU data memory located at XDATA space and MCU uses it to store data in process.

5.11 GPIO and PWM

Two PWM signal generators which can be used to control LED flashing behavior. There are also some GPIO signals that can be controlled directly by MCU. These signals are multiplexed with peripherals. If some peripherals are turned on, the GPIO signals which is multiplexed will be disabled and these signals change to peripheral signals.

5.12 I2C Master

The I2C Master controller can be used to access external I2C slave device.

5.13 DMA

The DMA controller use to transfer data between Flexible DMA FIFO and XDATA RAM. MCU can control this DMA to get data from FIFO or to put data to FIFO from XDATA RAM. It can also be used to transfer data between P-RAM to SPI flash controller or eMMC flash controller.

5.14 SPI Flash Controller

SPI Flash Controller can be used to access data of SPI serial flash memory. It can support single data bit, dual data bits and quad data bits SPI serial flash memory. The data can be transferred to FIFO or XDATA RAM.

5.15 eMMC Controller

eMMC Controller can be used to access external eMMC flash memory. It can support single data bit and quad data bit modes. The data of eMMC flash memory can be transferred to FIFO or XDATA RAM.

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 6-1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{CCK}	1.2V Core Power Supply	-0.3 to 1.4	V
V_{CC}	3.3V Power Supply	-0.3 to 4.0	V
V_{D5}	5V Power Supply	-0.3 to 6.0	V
V_{IN3}	Input Voltage of 3.3V I/O	-0.3 to V_{CC3I} +0.3	V
	Input Voltage of 3.3V I/O with 5V Tolerance	-0.3 to 5.5	
T_{STG}	Storage Temperature	-40 to 150	^{o}C

6.2 Recommended Operating Conditions

Table 6-2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{D5}	5V Power Supply	4.5	5	5.5	V
V_{CCK}	1.2V Core Power Supply	1.14	1.2	1.26	V
V_{CC3I}	Power Supply of 3.3V I/O	3.0	3.3	3.6	V
T	Operating Temperature	0	25	70	^{o}C

6.3 Recommended Operating Conditions of 3.3V GPIO

Table 6-3 Recommended Operating Conditions of 3.3V GPIO

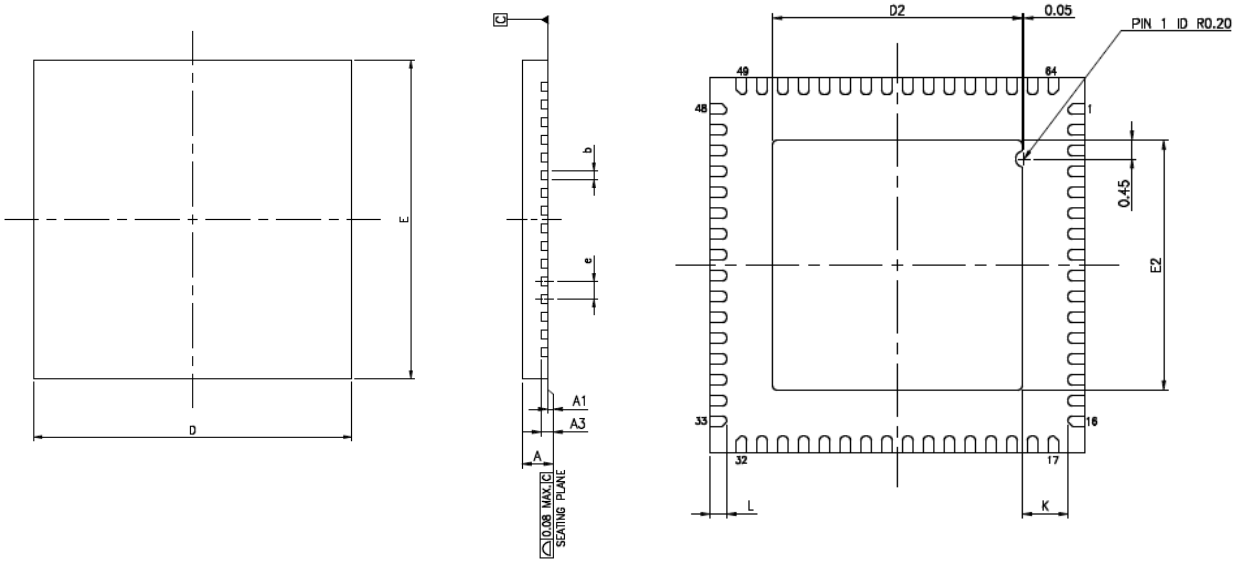
Symbol	Parameter	Min	Typ	Max	Units
V_{DD33}	I/O Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0		5.5	V
V_{IL}	Input Low Voltage	-0.3		0.8	V
R_{PU}	Pull-up Resistor	62	77	112	kΩ
V_{OL}	Output Low Voltage			0.4	V
V_{OH}	Output High Voltage	2.4			V
I_{OL}	Low Level Output Current @V_{OL} =0.4V	8			mA
I_{OH}	High Level Output Current @V_{OL} =2.4V	12			mA

6.4 Operating Current

Table 6-4 Operating Current

Symbol	Parameter	Connection	Current of 3.3V	Current of 1.2V	Units
I_{DD}	Operating Current	USB 3.0	70	246	mA
		USB 2.0	62	93	mA
I_{SUS}	Suspend Current (Sleep, bus-powered)	USB 3.0	0.17	0.9	mA
		USB 2.0	0.4	0.75	mA

7. Outline Diagram



	PACKAGE TYPE		
JEDEC OUTLINE	MO-220		
PKG CODE	VQFN (Y964)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
B	0.18	0.25	0.30
D	9.00 BSC		
E	9.00 BSC		
e	0.50 BSC		
K	0.20	-	-

	E2			D2			L			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
244x244 MIL	5.90	6.00	6.05	5.90	6.00	6.05	0.35	0.40	0.45	V	X	(V) WMMD-4

NOTES:

1. All dimensions are in millimeters.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

Figure 7-1 Outline Diagram of QFN64

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