PL2701 / PL27A1

SuperSpeed USB Host-to-Host Bridge Controller

USB PCB Layout Guide

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Prolific Technology Inc.
7F, No. 48, Sec. 3, Nan Kang Rd.
Nan Kang, Taipei 115, Taiwan, R.O.C.
Telephone: +886-2-2654-6363
Fax: +886-2-2654-6161
E-mail: sales@prolific.com.tw
Website: http://www.prolific.com.tw

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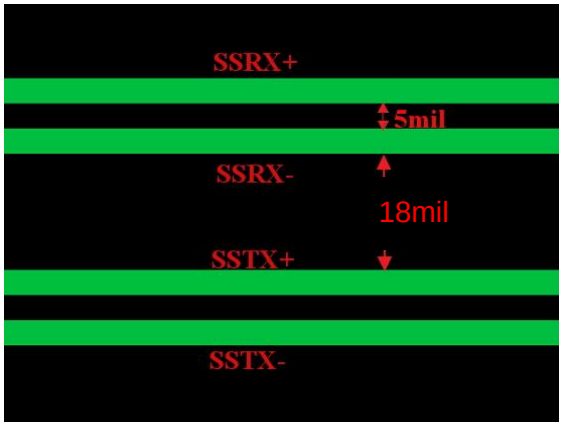
1. Overview

This document explains how to design a PCB for Prolific PL2701/PL27A1 SuperSpeed USB 3.0 Host to Host Bridge Controller device.

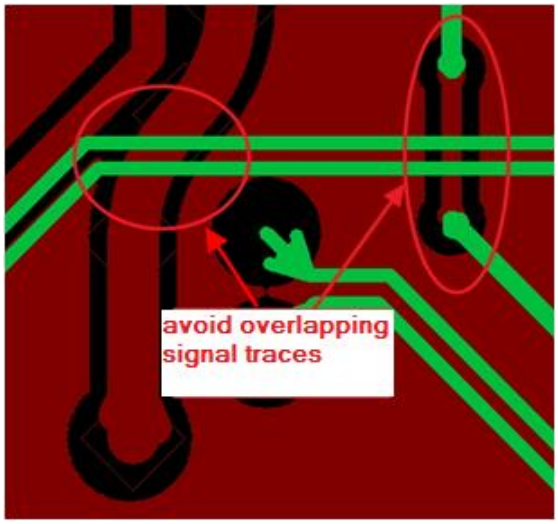
2. USB 3.0 Trace

- USB 3.0 consists of two differential pair traces, a transmit pair (SSTX+ and SSTX-) and a receive pair (SSRX+ and SSRX-). Each differential pair traces should be routed with differential impedance of 90±7 ohms.

- The spacing between the two traces of each differential pair should be 5 mils. The spacing between the two differential pairs (a transmit pair and a receive pair) should be 18 mils shown in Figure below. The spacing between each differential pair and other signals or ground traces or ground planes should be 20 mils for preventing crosstalk.



- Never route USB 3.0 differential trace over split ground and power planes. A bad example is shown in Figure below where the USB3.0 differential pair is routed on the top layer of PCB and overlapping the split ground plane with other signal traces on the second layer (for 4-layer) or the bottom layer (for 2-layer) of the PCB.



- The spacing between each differential pair and power trace or plane should be 20 mils.

- The spacing between two USB 3.0 differential pairs and a USB 2.0 differential pairs should be 20 mils or implemented with ground plane.

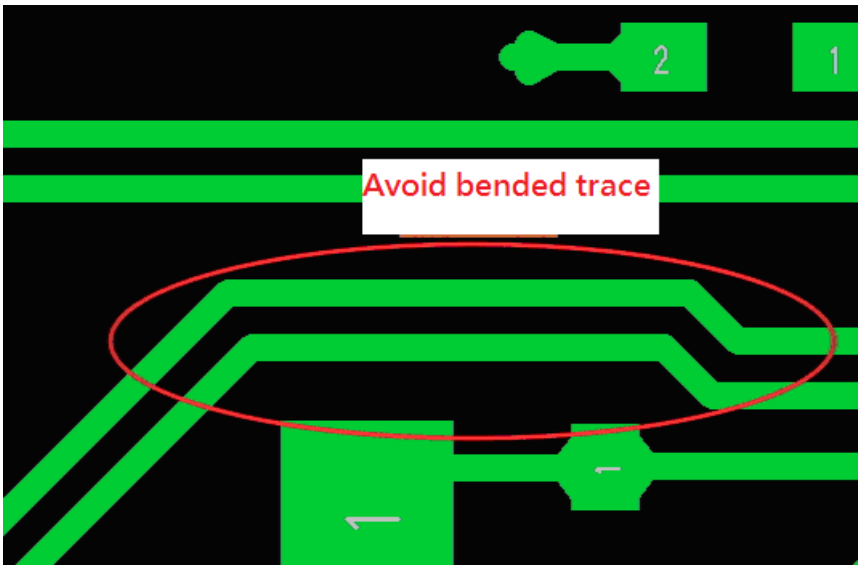
- The length of one trace of each differential pair should be as same as possible with another trace.

- It is permissible to swap the plus and minus traces on one or both of the USB 3.0 differential pairs. This may be useful to prevent the differential traces from crossing over one another. However, it is not permissible to swap the transmitter differential pair with the receiver differential pair.

- When using the common mode choke for reducing EMI and ESD clamper, they should be placed as close as possible to the USB 3.0 connector.

- The transmitter differential pair requires two 0.1 µF coupling capacitors for proper operation. The package size of these capacitors should be no bigger than 0402 and 0603 and placed symmetrically as close as possible to the USB 3.0 connector signal pins.

- It is recommended to use straight routes for USB 3.0 differential pairs rather than bending routes as shown in Figure below.



3. USB 2.0 Trace

- USB 2.0 differential pair traces should be routed with differential impedance of 90±15% ohms (single ended impedance of 45 ohms).

- The length of one trace of USB 2.0 differential pair should be as same as possible with another trace.

- When using common mode choke for reducing EMI and ESD clamper, they should be placed as close as possible to the USB3.0 connector.

4. Power Supply

- To maintain voltage stability, the bypass capacitors for the analog 1.2V power supply pin (pin8, 14, 40, 46) of PL2701/PL27A1 should be as close as possible to the PL2701/PL27A1 IC, and the cascaded FB (ferrite beads) for the analog 1.2V power supply pin are recommended to use 1A or above, with impedance of 600ohms @ 100MHz, and 60mV specifications (e.g. model LCB1608K-601T20).

- The two feedback resistors of the voltage feedback pin (VFB) of the 1.2V DC-DC converter should be as close to the VFB pin. This ensures the accuracy of the output voltage (Note: The 1.2V voltage range requirement of PL2701/25B1 is 1.14 ~ 1.26V).

- Never route any GND trace between the two pins of the power choke for the 1.2V DC-DC converter. The spacing between two pins of the power choke and surrounding ground plane or trace should be 20 mils.

5. Others

- The pins USB_VBUS (pin 25) and USB_VBUS1 (pin 26) of the PL2701/PL27A1 IC are signal pins used to detect the connection between the PL2701/PL27A1 and the USB host controller. Thus, the trace width of pins USB_VBUS and USB_VBUS1 do not have certain requirement.

- The two NC pins of the 4-pin SMD crystal should be connected to ground for reducing EMI.

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7F, No. 48, Sec. 3, Nan Kang Rd.

Nan Kang, Taipei 115, Taiwan, R.O.C.

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